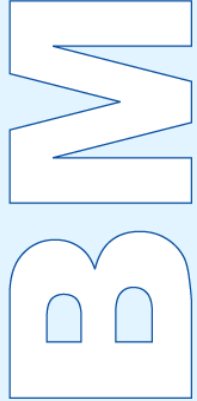




# MiDAS Family

**BM-MiDAS2.1-V1.8**



## Brief Manual of MiDAS2.1 Family

### FLASH / ISP / IAP 8-bit Turbo Microcontrollers

V1.8

April 2008

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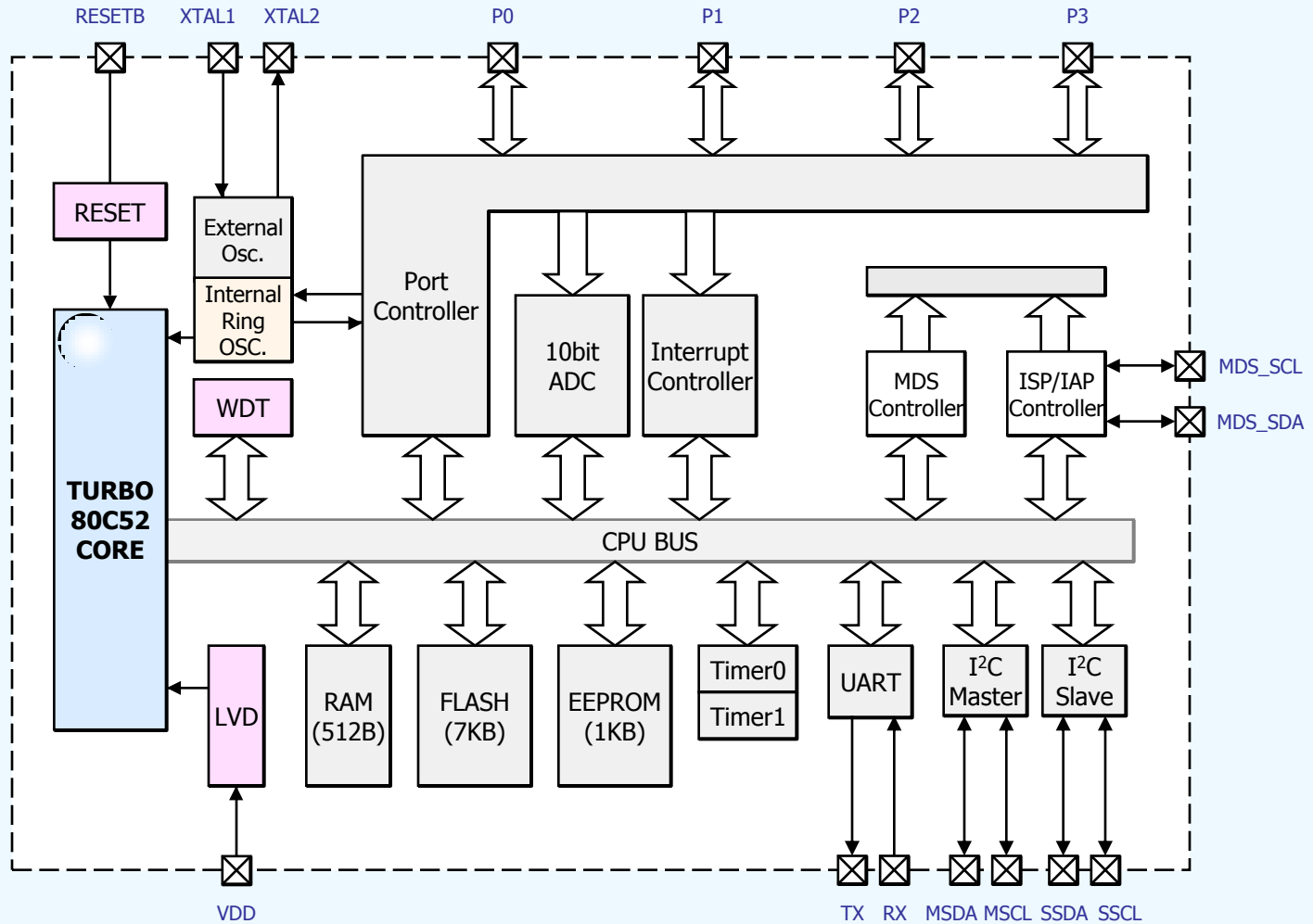
# 1. Product Overview

- ◆ **CORERIVER's MiDAS2.1 Family is a group of fast 80C52 compatible microcontrollers**
- ◆ **The instruction execution is max. 3 times faster than that of traditional 80C52.**
  - ✓ 1 Machine cycle = 4 clocks vs. 12 clocks
- ◆ **Additional peripherals of MiDAS2.1 Family:**
  - ✓ 10 bit ADC / 8-bit PWM / I<sup>2</sup>C / UART / WDT / LVD / POR.
- ◆ **Power saving modes**
- ◆ **Noise tolerant scheme**
- ◆ **Support ISP / IAP of FLASH memory**
- ◆ **Provides User-Friendly MDS environment with on-chip HW debug engine**
- ◆ **Provides Easy-to-Use training-kit system**

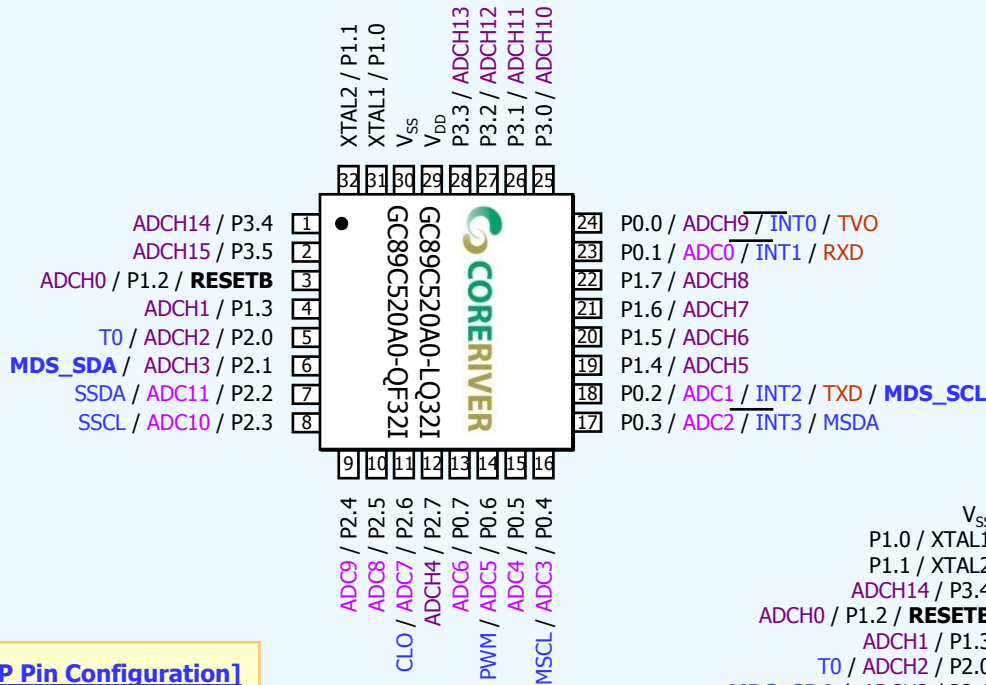
## 2. Features

- ◆ CPU
  - ✓ 8-bit turbo 80C52 architecture
  - ✓ 4 cycles/1 machine cycle
  - ✓ instruction level compatible with Intel 80C52
- ◆ 7 KBytes FLASH + 1 KByte User EEPROM
- ◆ 512 Bytes RAM
- ◆ Operating Voltage : 2.2V ~ 5.5V
- ◆ Operating Frequency
  - ✓ Max. 20MHz @4.5V ~ 5.5V
  - ✓ Max. 12MHz @2.2V ~ 3.3V
- ◆ Operating Temperature : -40 °C to 120 °C
- ◆ Max. Programmable 30 I/O Pins
  - ✓ Pull-up control, Open drain, Push-Pull output
- ◆ TTL and CMOS compatible logic levels
- ◆ Low Voltage Detector
- ◆ Internal Ring OSC. : 12MHz@3V(+/-1%)
- ◆ 28-channel 10-bit ADC
  - ✓ Max 100KSPS (@F<sub>ADC</sub> = 10 MHz)
  - ✓ Programmable input clock frequency
- ◆ Two 16-bit Timer/Counter
- ◆ 1-channel 8-bit high speed PWM
- ◆ 16-bit Programmable Watchdog Timer
- ◆ I<sup>2</sup>C Master / Slave
- ◆ 13 Interrupt Sources
  - ✓ Timer0/1, UART, WDT, PWM, LVD, ADC, 2-I<sup>2</sup>C, & 4 External
  - ✓ Two-level interrupt priority
- ◆ Reset Scheme
  - ✓ On-chip power-on-reset
  - ✓ External reset
  - ✓ Low voltage detector reset
  - ✓ Watchdog timer reset (optional)
- ◆ Power Consumption
  - ✓ active current : Max 8mA @3V, 12MHz
  - ✓ idle current : Max 3mA @3V, 12MHz
  - ✓ stop current : Typ. < 0.1uA @2.2V  
Max 1uA @ 5V
- ◆ E.S.D. Protection Up to 2,000V
- ◆ Latch-up Protection Up to ±200mA
- ◆ Package : 32-LQFP (TQFP) / 28-SOIC / 32-QFN

# 3. Block Diagram








# 4. Pin configuration

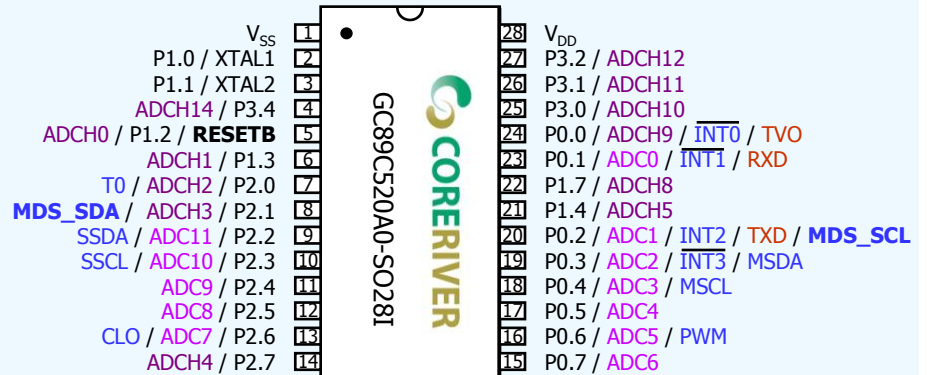


[ 32-LQFP / 32-QFN ]

**[ISP Pin Configuration]**

-  V<sub>DD</sub> (+3.3V)
-  V<sub>SS</sub> (GND)
-  MDS\_SCL (P0.2)
-  RESETB (P1.2)
-  MDS\_SDA (P2.1)

- ◆ If the operating voltage of target board is +5V, don't connect V<sub>DD</sub> cable pin of GenICE52 equipment.
- ◆ Please, individually supply the voltage (+5V) to target board.
- ◆ The other cable pins of GenICE52 are +5V compatible.



[ 28-SOIC ]

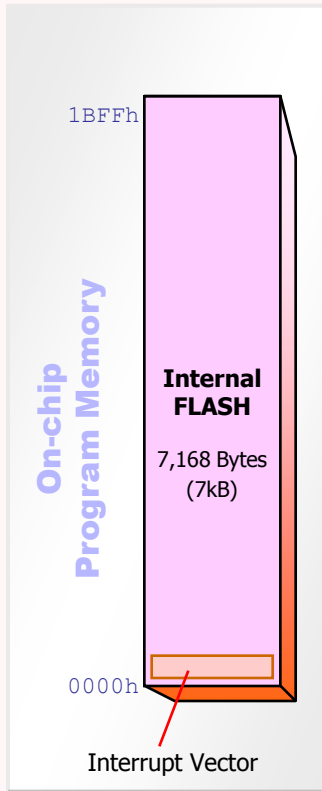
## 5. Pin Descriptions

Symbol	Direction	Description	Share Pins
$V_{DD}$	Input	Power Supply	-
$V_{SS}$	Input	Ground	-
XTAL1 / P1.0	Input/Output	<ul style="list-style-type: none"> <li>▪ Crystal Input/Output (Default)</li> <li>▪ Bit Programmable with Schmitt Trigger                             <ul style="list-style-type: none"> <li>- Optional Pull-up Control Enable</li> <li>- Open-drain Output</li> <li>- Push-pull Output</li> </ul> </li> </ul>	XTAL1 / P1.0 (Crystal Input)
XTAL2 / P1.1			XTAL2 / P1.1 (Crystal Output)
RESETB / P1.2	Input/Output	<ul style="list-style-type: none"> <li>▪ External Reset Input Signal (Default)</li> <li>▪ Bit Programmable                             <ul style="list-style-type: none"> <li>- Optional Pull-up Control Enable</li> <li>- Open-drain Output</li> <li>- Push-pull Output</li> </ul> </li> </ul>	<b>RESETB</b> / P1.2 / <b>ADCH0</b>
P1[7:3]	Input/Output	<ul style="list-style-type: none"> <li>▪ Bit Programmable with Schmitt Trigger                             <ul style="list-style-type: none"> <li>- Optional Pull-up Control Enable</li> <li>- Open-drain Output</li> <li>- Push-pull Output (Default)</li> </ul> </li> </ul>	P1.3 / <b>ADCH1</b> P1.4 / <b>ADCH5</b> P1.5 / <b>ADCH6</b> P1.6 / <b>ADCH7</b> P1.7 / <b>ADCH8</b>
P0[7:0]	Input/Output	<ul style="list-style-type: none"> <li>▪ Bit Programmable with Schmitt Trigger                             <ul style="list-style-type: none"> <li>- Optional Pull-up Control Enable</li> <li>- Open-drain Output</li> <li>- Push-pull Output (Default)</li> </ul> </li> </ul>	P0.0 / <b>ADCH9</b> / <b>INT0</b> / <b>TVO</b> P0.1 / <b>ADC0</b> / <b>INT1</b> / <b>RXD</b> P0.2 / <b>ADC1</b> / <b>INT2</b> / <b>TXD</b> / <b>MDS_SCL</b> P0.3 / <b>ADC2</b> / <b>INT3</b> / <b>MSDA</b> P0.4 / <b>ADC3</b> / <b>MSCL</b> P0.5 / <b>ADC4</b> P0.6 / <b>ADC5</b> / <b>PWM</b> P0.7 / <b>ADC6</b>

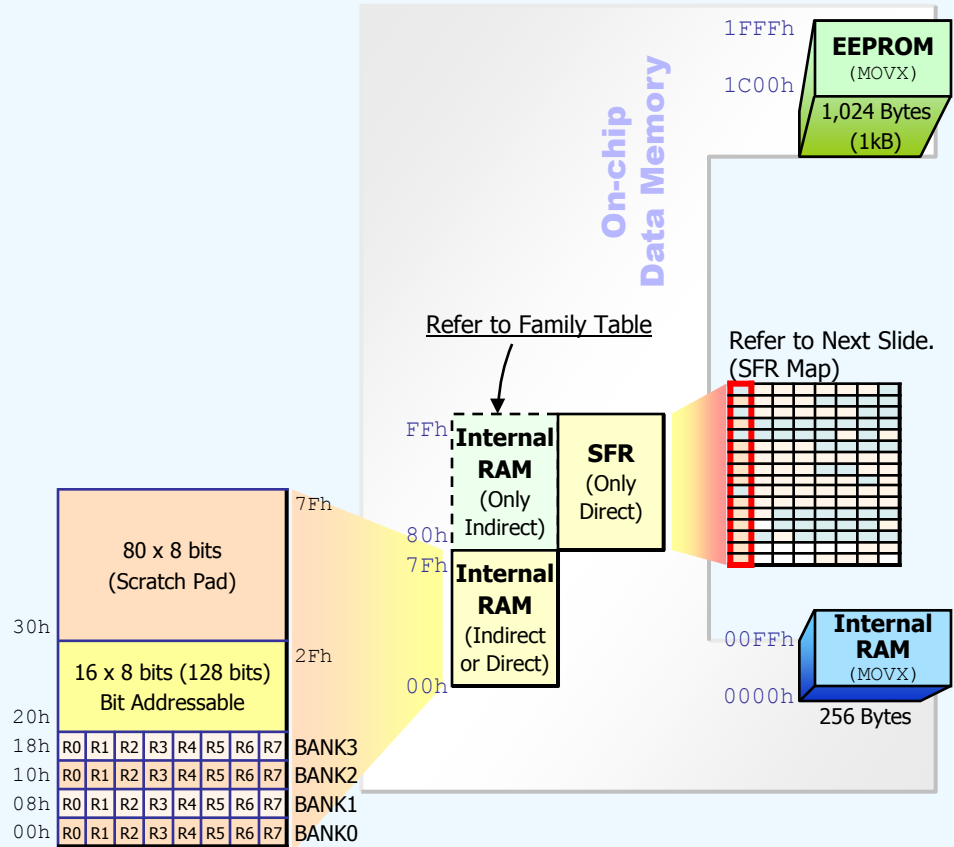
## 5. Pin Descriptions (Cont'd)

Symbol	Direction	Description	Share Pins
P2[7:0]	Input/Output	<ul style="list-style-type: none"> <li>▪ Bit Programmable with Schmitt Trigger</li> <li>- Optional Pull-up Control Enable</li> <li>- Open-drain Output</li> <li>- Push-pull Output (Default)</li> </ul>	P2.0 / ADCH2 / T0 P2.1 / ADCH3 / <b>MDS_SDA</b> P2.2 / ADC11 / SSSDA P2.3 / ADC10 / SSCL P2.4 / ADC9 P2.5 / ADC8 P2.6 / ADC7 / CLO P2.7 / ADCH4
P3[5:0]	Input/Output	<ul style="list-style-type: none"> <li>▪ Bit Programmable with Schmitt Trigger</li> <li>- Optional Pull-up Control Enable</li> <li>- Open-drain Output</li> <li>- Push-pull Output (Default)</li> </ul>	P3.0 / ADCH10 P3.1 / ADCH11 P3.2 / ADCH12 P3.3 / ADCH13 P3.4 / ADCH14 P3.5 / ADCH15

# 6.1. Memory Organization



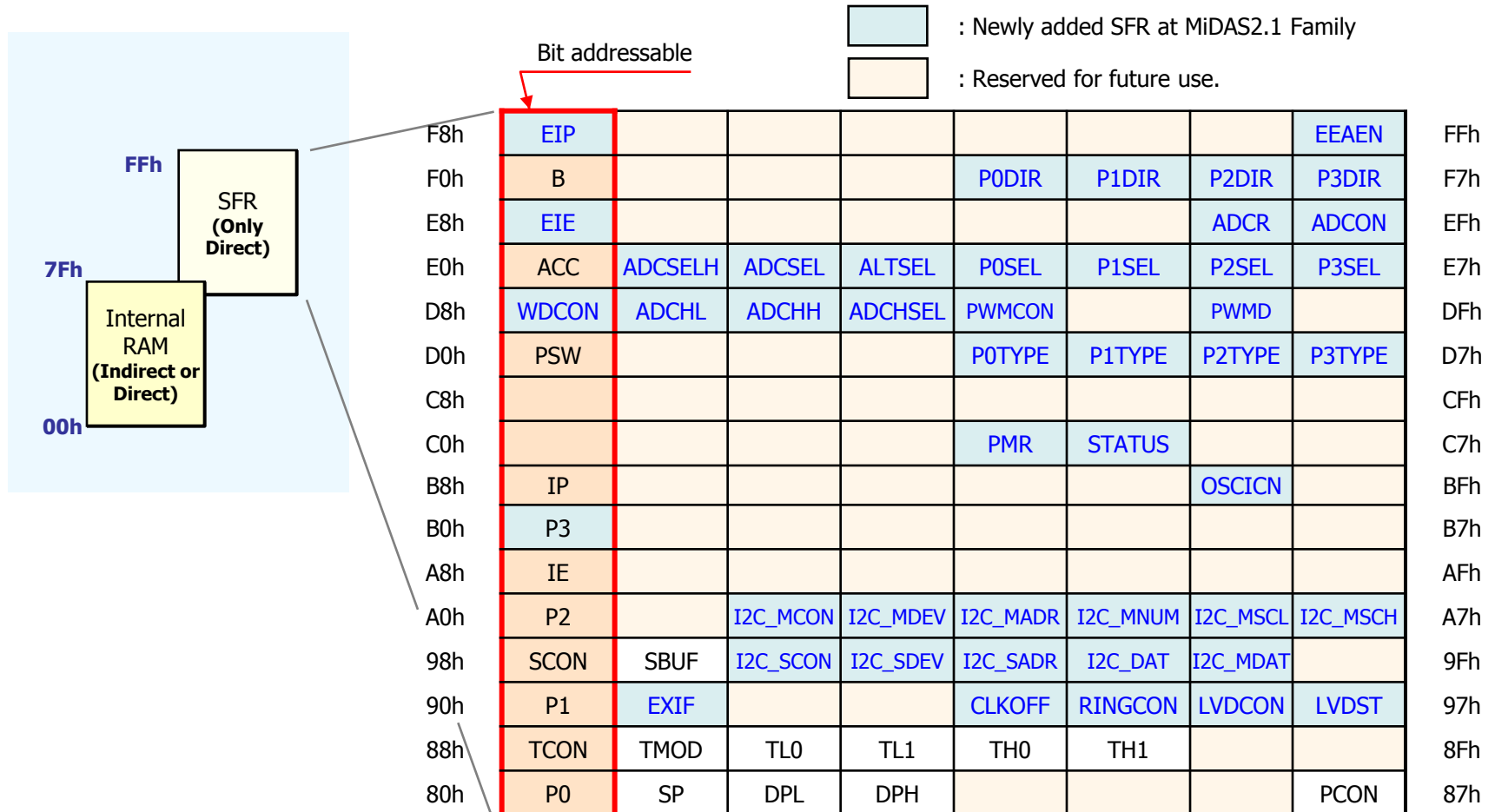
[ On-chip Program Memory ]  
(Read/Write with IAP)



[ On-chip Data Memory ]  
(Read and Write)

◆ User can write the data to FLASH or EEPROM with IAP (In-Application Programming).

## 6.2. SFR (Special Function Register) Map



## 6.2. SFR Brief Description

### ◆ 80C52 SFR Registers

Register	Name	Reset Value
<b>ACC</b> <b>B</b> <b>PSW</b> <b>SP</b>	Accumulator B Program Status Word Stack Pointer	00000000 00000000 00000000 00001111
<b>DPTR</b> <b>DPL</b> <b>DPH</b>	Data Pointer (2 bytes) Low Byte High Byte	00000000 00000000
<b>P0</b> <b>P1</b> <b>P2</b> <b>P3</b>	Port 0 Port 1 Port 2 Port 3	11111111 11111111 11111111 **111111
<b>IP</b> <b>IE</b>	Interrupt Priority Interrupt Enable Control	10*00000 00*00000
<b>TCON</b> <b>TMOD</b>	Timer/Counter 0/1 Control Timer/Counter 0 Mode Control	00000000 ****0000
<b>TH0</b> <b>TL0</b> <b>TH1</b> <b>TL1</b>	Timer/Counter 0 High Byte Timer/Counter 0 Low Byte Timer/Counter 1 High Byte Timer/Counter 1 Low Byte	00000000 00000000 00000000 00000000
<b>SCON</b> <b>SBUF</b>	Serial Control Serial Buffer	***0**00 00000000
<b>PCON</b>	Power Control	0**10000

### ◆ Newly added SFR Registers at MiDAS2.1 Family

Register	Name	Reset Value
<b>P0SEL</b> <b>P1SEL</b> <b>P2SEL</b> <b>P3SEL</b>	Port 0 Pull-up Control Port 1 Pull-up Control Port 2 Pull-up Control Port 3 Pull-up Control	00000000 00000011 00000000 **000000
<b>P0TYPE</b> <b>P1TYPE</b> <b>P2TYPE</b> <b>P3TYPE</b>	Port 0 Type Control Port 1 Type Control Port 2 Type Control Port 3 Type Control	00000000 00000000 00000000 **000000
<b>P0DIR</b> <b>P1DIR</b> <b>P2DIR</b> <b>P3DIR</b>	Port 0 Input/Output Control Port 1 Input/Output Control Port 2 Input/Output Control Port 3 Input/Output Control	11111111 11111111 11111111 **111111
<b>ALTSEL</b>	Alternative Function Control	000000**
<b>PWMCON</b> <b>PWMD</b>	PWM Control PWM Duty Data	0000*000 00000000
<b>ADCON</b> <b>ADCR</b> <b>ADCSEL</b> <b>ADCSELH</b> <b>ADCHL</b> <b>ADCHH</b> <b>ADCHSEL</b>	ADC Control & ADC Result Low ADC Result High ADC Channel Selection Low and MUX Selection ADC Channel Selection High ADC High Channel Selection High ADC High Channel Selection Low ADC High Channel Selection	0010*000 00000000 11111111 11111111 11111111 11111111 0***0000
<b>EEAEN</b>	EEPROM Access Enable	*****0

\* : Don't touch bit.

## 6.2. SFR Brief Description (Cont'd)

### ◆ Newly added SFR Registers at MiDAS2.1 Family (Cont'd)

Register	Name	Reset Value
<b>WDCON</b>	Watchdog Timer Control	11010000
<b>PMR</b>	Power Management Control	****0***
<b>EXIF</b>	Added External Interrupt and LVD Control	**000101
<b>EIP</b>	Extended Interrupt Priority	**00**00
<b>EIE</b>	Extended Interrupt Enable	**00**00
<b>STATUS</b>	Crystal Status	***0****
<b>OSCICN</b>	Internal Ring Oscillator Control	****1100
<b>CLKOFF</b>	Clock Control for Minimizing Power Consumption	**00*000
<b>RINGCON</b>	Internal Ring Oscillator Tuning	01100000
<b>LVDCON</b>	Power Fail Interrupt Source Selection	*****000
<b>LVDST</b>	Current Power Supply Status	00000000
<b>I2C_MCON</b>	I <sup>2</sup> C Master Control	***00000
<b>I2C_MDEV</b>	I <sup>2</sup> C Master Device Address	00000000
<b>I2C_MADR</b>	I <sup>2</sup> C Master Memory Address	00000000
<b>I2C_MNUM</b>	I <sup>2</sup> C Master Multi-byte Number	00000000
<b>I2C_MSCL</b>	I <sup>2</sup> C Master Clock Scale Factor Low Byte	00000000
<b>I2C_MSCH</b>	I <sup>2</sup> C Master Clock Scale Factor High Byte	00000000
<b>I2C_MDAT</b>	I <sup>2</sup> C Master Data	00000000
<b>I2C_SCON</b>	I <sup>2</sup> C Slave Control	*000*000
<b>I2C_SDEV</b>	I <sup>2</sup> C Slave Device Address	00000000
<b>I2C_SADR</b>	I <sup>2</sup> C Slave Memory Address	00000000
<b>I2C_SDAT</b>	I <sup>2</sup> C Slave Data	00000000

\* : Don't touch bit.

## 6.3. Instruction Set Summary

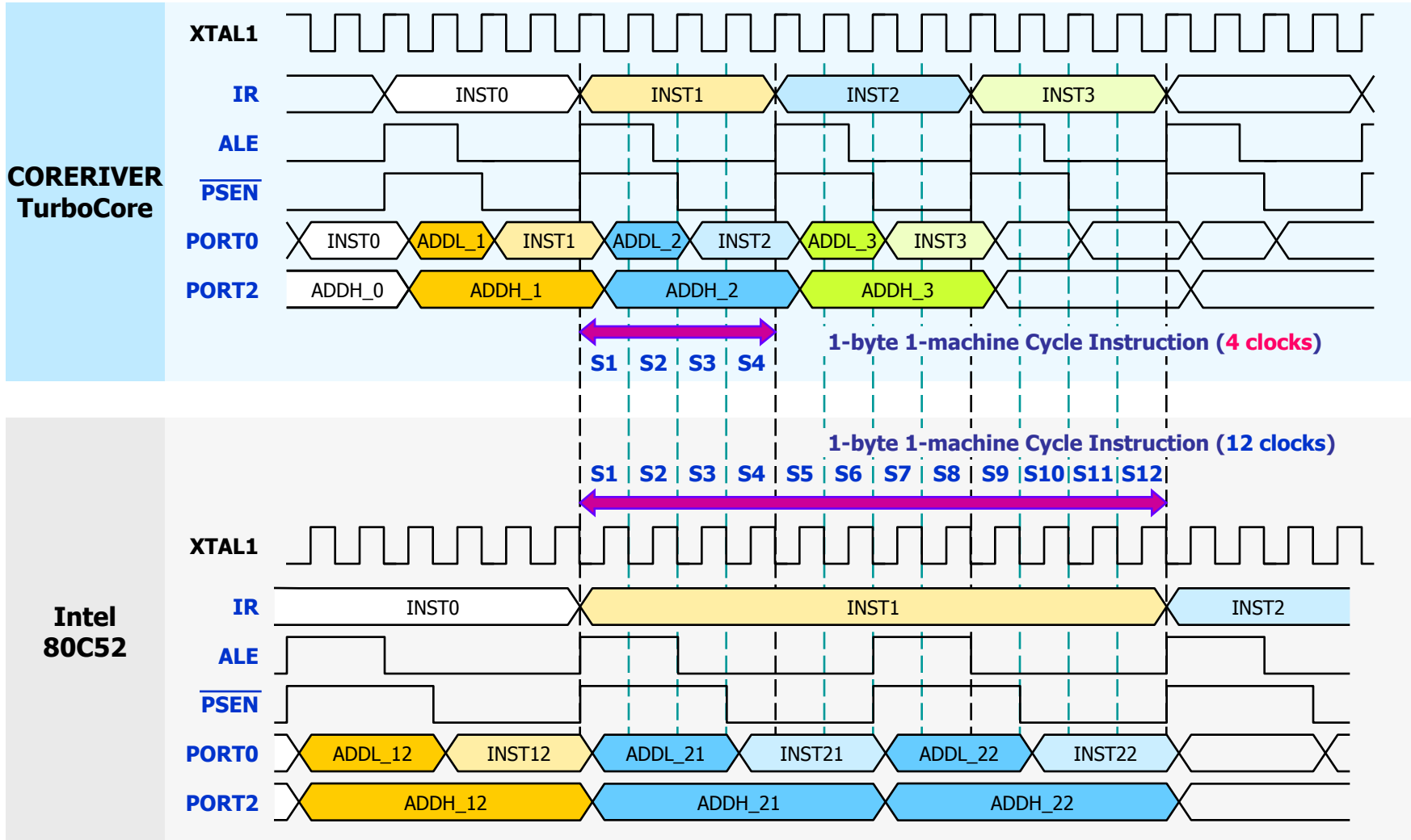
- ◆ Refer to Appendix A (Instruction Set) for more details.

Type	Instruction	Description
Arithmetic	ADD	Addition
	ADDC	Addition with Carry
	SUBB	Subtraction with Borrow
	INC	Increment
	DEC	Decrement
	MUL	Multiply
	DIV	Divide
	DA	Decimal Adjust
Logical	ANL	AND
	ORL	OR
	XRL	Exclusive OR
	CLR	Clear
	CPL	Complement
	RL	Rotate Left
	RLC	Rotate Left with Carry
	RR	Rotate Right
	RRC	Rotate Right with Carry
SWAP	Swap Nibbles	
Data Transfer	MOV	Move Data
	MOVC	Move Code
	MOVX	Move Data to Ext. RAM
	PUSH	PUSH
	POP	POP
	XCH	Exchange
	XCHD	Exchange Low-digit

Type	Instruction	Description
Boolean	CLR	Clear bit
	SETB	Set bit
	CPL	Complement bit
	ANL	AND bit
	ORL	OR bit
	MOV	Move bit
	JC	Jump if Carry is set
	JNC	Jump if Carry is not set
	JB	Jump if bit is set
	JNB	Jump if bit is not set
JBC	Jump if bit is set & clear	
Branch	ACALL	Absolute Call
	LCALL	Long Call
	RET	Return from Subroutine
	RETI	Return from Interrupt
	AJMP	Absolute Jump
	LJMP	Long Jump
	SJMP	Short Jump
	JMP	Jump with DPTR
	JZ	Jump if ACC is zero
	JNZ	Jump if ACC is not zero
CJNE	CJNE	Compare and Jump if not equal
	DJNZ	Decrement and Jump if not zero
	NOP	No Operation

## 6.4. CPU Timing

- ◆ Comparative timing of the MiDAS2.1 family and Intel 80C52



## 6.4. CPU Timing : Execution Time Table

- ◆ The fastest instruction execution in the world

Instruction	Turbo Core (CORERIVER)	W77C32 (Winbond)	DS80C320 (Maxim)	87C52 (Intel)
MUL AB DIV AB	<b>12 clocks</b>	20 clocks	20 clocks	48 clocks
MOVC A, @A+PC MOVC A, @A+DPTR	<b>8 clocks</b>	8 clocks	12 clocks	24 clocks
JMP @A+DPTR	<b>8 clocks</b>	8 clocks	12 clocks	24 clocks
RET RETI	<b>8 clocks</b>	8 clocks	16 clocks	24 clocks
INC DPTR DEC DPTR	<b>4 clocks</b> <b>4 clocks</b>	8 clocks 8 clocks	12 clocks Not exist	24 clocks Not exist
Others	<b>Same</b>	Same	Same	-

## 6.5. I/O Ports : PORT0[7:0]

- ◆ Push-pull output type with enabled pull-ups by default.
- ◆ P0[7:0] can be configured as ADC input : ADC6 (P0.7) ~ ADC0 (P0.1) and ADCH9 (P0.0).
- ◆ Read-Modify-Write instructions do not read port pin but SFR register.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y

### ✓ P0TYPE (D4h) : Port 0 Type Control Register

P0TYPE.7	P0TYPE.6	P0TYPE.5	P0TYPE.4	P0TYPE.3	P0TYPE.2	P0TYPE.1	P0TYPE.0
----------	----------	----------	----------	----------	----------	----------	----------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- 0 = Push-pull Output (Default) / 1 = Open-drain Output

### ✓ PODIR (F4h) : Port 0 Input/Output Control Register

PODIR.7	PODIR.6	PODIR.5	PODIR.4	PODIR.3	PODIR.2	PODIR.1	PODIR.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- 0 = Output / 1 = Input (Default)

### ✓ POSEL (E4h) : Port 0 Pull-up Control Register

POSEL.7	POSEL.6	POSEL.5	POSEL.4	POSEL.3	POSEL.2	POSEL.1	POSEL.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

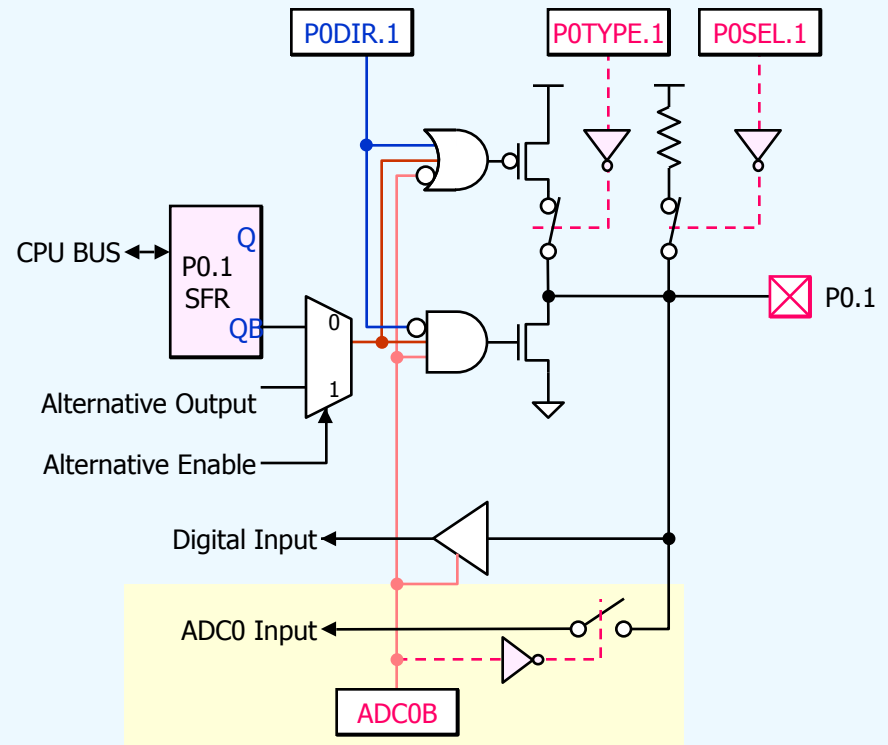
- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC\_EN (ADCON[7]) = 1

### ✓ P0 (80h) : Port 0 Register

P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
------	------	------	------	------	------	------	------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ✓ ADCSEL (E2h), ADCSELH (E1h), and ADCHH(DA)  
: Refer to Next Slide



## 6.5. I/O Ports : PORT0[7:0] (Cont'd)

- ✓ **ADCSEL** (E2h) : ADC Channel Selection Low & MUX Selection

ADC3B	ADC2B	ADC1B	ADC0B	CH3	CH2	CH1	CH0
-------	-------	-------	-------	-----	-----	-----	-----

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ADCXB = 0 : ADCX Input Enable & Digital Input Disable

- ✓ **ADCSELH** (E1h) : ADC Channel Selection High Register

ADC11B	ADC10B	ADC9B	ADC8B	ADC7B	ADC6B	ADC5B	ADC4B
--------	--------	-------	-------	-------	-------	-------	-------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ADCXB = 0 : ADCX Input Enable & Digital Input Disable

- ✓ **ADCHH** (DAh) : ADC High Channel Selection High Register

ADCH15B	ADCH14B	ADCH13B	ADCH12B	ADCH11B	ADCH10B	ADCH9B	ADCH8B
---------	---------	---------	---------	---------	---------	--------	--------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ADCHXB = 0 : ADCHX Input Enable & Digital Input Disable

## 6.5. I/O Ports : PORT1[1:0] (XTAL1/XTAL2)

- ◆ XTAL1/XTAL2 can be configured as I/O port.
- ◆ Read-Modify-Write instructions do not read port pin but SFR register.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y

### ✓ P1TYPE (D5h) : Port 1 Type Control Register

P1TYPE.7	P1TYPE.6	P1TYPE.5	P1TYPE.4	P1TYPE.3	P1TYPE.2	P1TYPE.1	P1TYPE.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Push-pull Output (Default) / 1 = Open-drain Output

### ✓ P1DIR (F5h) : Port 1 Input/Output Control Register

P1DIR.7	P1DIR.6	P1DIR.5	P1DIR.4	P1DIR.3	P1DIR.2	P1DIR.1	P1DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Output / 1 = Input (Default)

### ✓ P1SEL (E5h) : Port 1 Pull-up Control Register

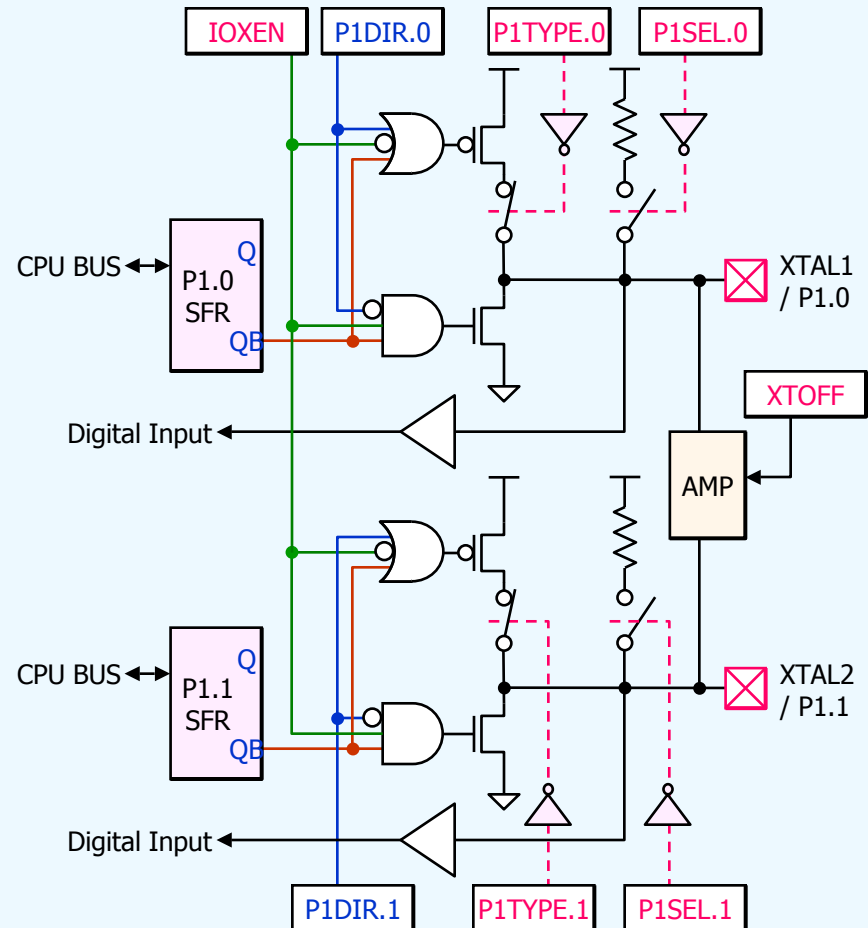
P1SEL.7	P1SEL.6	P1SEL.5	P1SEL.4	P1SEL.3	P1SEL.2	P1SEL.1	P1SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R/W(1)

- 0 = Pull-up resistor ON
- 1 = Pull-up resistor OFF (Default) when ADC\_EN (ADCON[7]) = 1

### ✓ P1 (90h) : Port 1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ✓ **ALTSEL** (E3h), **PMR** (C4h), **STATUS** (C5h), and **EXIF** (91h) : Refer to Next Slide



## 6.5. I/O Ports : PORT1[1:0] (XTAL1/XTAL2) (Cont'd)

### ✓ **ALTSEL** (E3h) : Alternative Function Control Register

IOXEN	IORSTEN	CLO	PWM00	TV0	TX	-	-
-------	---------	-----	-------	-----	----	---	---

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- IOXEN = 1 : XTAL1 and XTAL2 are configured as I/O Ports

### ✓ **PMR** (C4h) : Power Management Control Register

-	-	-	-	XTOFF	-	-	-
---	---	---	---	-------	---	---	---

R/W(0)

- XTOFF : Internal amplifier disable for external crystal oscillator.  
1 = External crystal will be killed.  
0 = External crystal will run (Default).  
Don't set XTOFF bit to 1 when XT/RG = 1.

### ✓ **STATUS** (C5h) : Crystal Status Register

-	-	-	XTUP	-	-	-	-
---	---	---	------	---	---	---	---

R(0)

- XTUP : Crystal oscillator warm-up status. (External crystal oscillator)  
It represents the crystal clock is stable (1) or not (0).  
Cleared by H/W when Power-on reset and all kinds of reset.  
Cleared by H/W when XTOFF bit is set.  
Cleared by during Power-down wake-up when  
XT/RG (EXIF.3) = 1.  
Set by H/W after XTAL stabilization time.

### ✓ **EXIF** (91h) : External Interrupt Flag Register

-	-	IE3	IE2	XT/RG	RGMD	RGSL	BGS
---	---	-----	-----	-------	------	------	-----

R/W(0) R/W(0) R/W(0) R(1) R/W(0) R/W(1)

- XT/RG : System clock selection.  
0 = Internal Ring oscillator is selected as system clock.  
1 = External clock is selected as system clock.

## 6.5. I/O Ports : PORT1[7:2]

- ◆ Push-pull output type with enabled pull-ups by default.
- ◆ P1[7:2] can be configured as ADC input : ADCH8 (P1.7) ~ ADCH5 (P1.4), ADCH1 (P1.3), and ADCH0 (P1.2).
- ◆ Read-Modify-Write instructions do not read port pin but SFR register.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y

### ✓ P1TYPE (D5h) : Port 1 Type Control Register

P1TYPE.7	P1TYPE.6	P1TYPE.5	P1TYPE.4	P1TYPE.3	P1TYPE.2	P1TYPE.1	P1TYPE.0
----------	----------	----------	----------	----------	----------	----------	----------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- 0 = Push-pull Output (Default) / 1 = Open-drain Output

### ✓ P1DIR (F5h) : Port 1 Input/Output Control Register

P1DIR.7	P1DIR.6	P1DIR.5	P1DIR.4	P1DIR.3	P1DIR.2	P1DIR.1	P1DIR.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- 0 = Output / 1 = Input (Default)

### ✓ P1SEL (E5h) : Port 1 Pull-up Control Register

P1SEL.7	P1SEL.6	P1SEL.5	P1SEL.4	P1SEL.3	P1SEL.2	P1SEL.1	P1SEL.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(1) R/W(1)

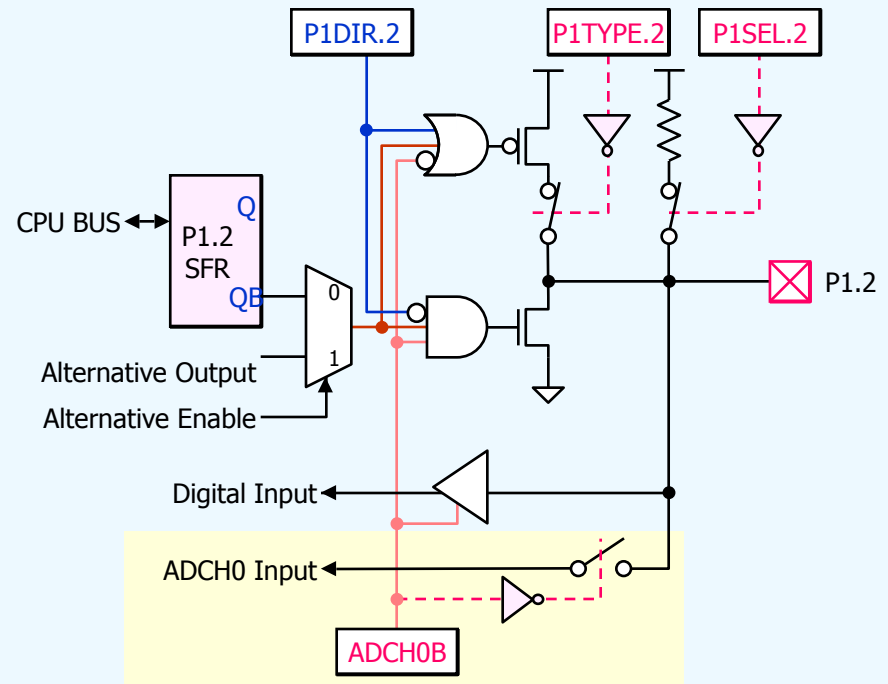
- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC\_EN (ADCON[7]) = 1

### ✓ P1 (90h) : Port 1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
------	------	------	------	------	------	------	------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ✓ ALTSEL (E3h), ADCHL(D9h), and ADCHH (DAh)  
: Refer to Next Slide



## 6.5. I/O Ports : PORT1[7:2] (Cont'd)

### ✓ **ALTSEL** (E3h) : Alternative Function Control Register

IOXEN	IORSTEN	CLO	PWM00	TV0	TX	-	-
-------	---------	-----	-------	-----	----	---	---

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- IORSTEN = 1 : RESETB is configured as I/O port.

### ✓ **ADCHL** (D9h) : ADC High Channel Selection Low Register

ADCH7B	ADCH6B	ADCH5B	ADCH4B	ADCH3B	ADCH2B	ADCH1B	ADCH0B
--------	--------	--------	--------	--------	--------	--------	--------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ADCHXB = 0 : ADCHX Input Enable (Digital Input Disable).

### ✓ **ADCHH** (DAh) : ADC High Channel Selection High Register

ADCH15B	ADCH14B	ADCH13B	ADCH12B	ADCH11B	ADCH10B	ADCH9B	ADCH8B
---------	---------	---------	---------	---------	---------	--------	--------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ADCHXB = 0 : ADCHX Input Enable (Digital Input Disable).

## 6.5. I/O Ports : PORT2[7:0]

- ◆ Push-pull type with enabled pull-ups by default.
- ◆ P2[7:0] can be configured as ADC input : ADCH4 (P2.7), ADC7 (P2.6) ~ ADC11 (P2.2), ADCH3 (P2.1), and ADCH2 (P2.0).
- ◆ Read-Modify-Write instructions do not read port pin but SFR register.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y

### ✓ P2TYPE (D6h) : Port 2 Type Control Register

P2TYPE.7	P2TYPE.6	P2TYPE.5	P2TYPE.4	P2TYPE.3	P2TYPE.2	P2TYPE.1	P2TYPE.0
----------	----------	----------	----------	----------	----------	----------	----------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- 0 = Push-pull Output (Default) / 1 = Open-drain Output

### ✓ P2DIR (F6h) : Port 2 Input/Output Control Register

P2DIR.7	P2DIR.6	P2DIR.5	P2DIR.4	P2DIR.3	P2DIR.2	P2DIR.1	P2DIR.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- 0 = Output / 1 = Input (Default)

### ✓ P2SEL (E6h) : Port 2 Pull-up Control Register

P2SEL.7	P2SEL.6	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	P2SEL.1	P2SEL.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

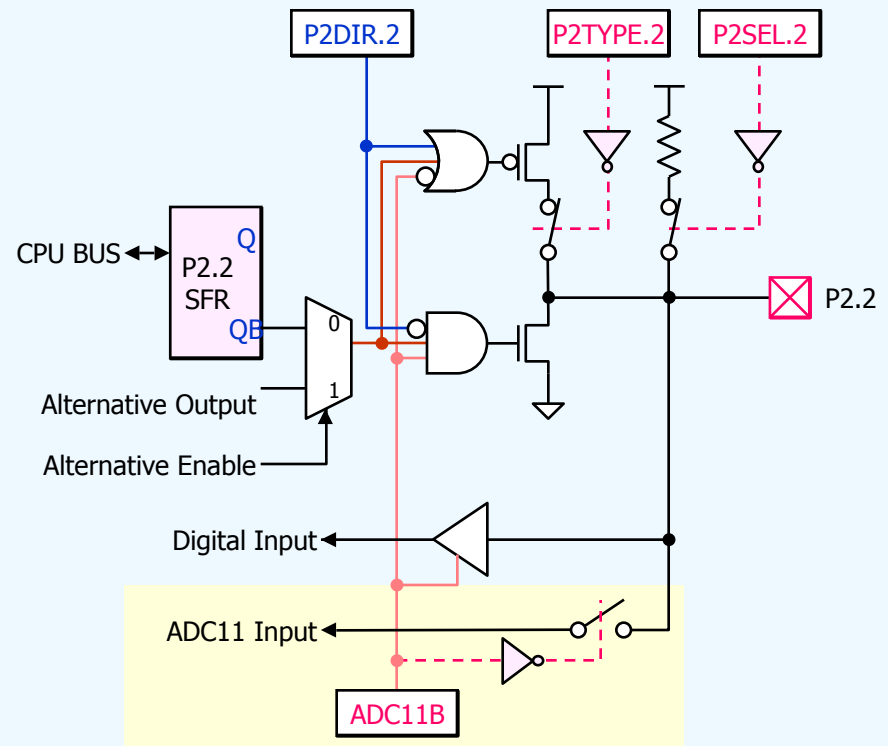
- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC\_EN (ADCON[7]) = 1

### ✓ P2 (A0h) : Port 2 Register

P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
------	------	------	------	------	------	------	------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

### ✓ ADCSELH (E1h), and ADCHL(D9) : Refer to Next Slide



## 6.5. I/O Ports : PORT2[7:0] (Cont'd)

### ✓ **ADCSELH** (E1h) : ADC Channel Selection High Register

ADC11B	ADC10B	ADC9B	ADC8B	ADC7B	ADC6B	ADC5B	ADC4B
--------	--------	-------	-------	-------	-------	-------	-------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ADCXB = 0 : ADCX Input Enable & Digital Input Disable

### ✓ **ADCHL** (D9h) : ADC High Channel Selection Low Register

ADCH7B	ADCH6B	ADCH5B	ADCH4B	ADCH3B	ADCH2B	ADCH1B	ADCH0B
--------	--------	--------	--------	--------	--------	--------	--------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ADCHXB = 0 : ADCHX Input Enable (Digital Input Disable).

## 6.5. I/O Ports : PORT3[5:0]

- ◆ Push-pull type with enabled pull-ups by default.
- ◆ P3[5:0] can be configured as ADC input : ADCH15 (P3.5) ~ ADCH10 (P3.0).
- ◆ Read-Modify-Write instructions do not read port pin but SFR register.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y

### ✓ P3TYPE (D7h) : Port 3 Type Control Register

-	-	P3TYPE.5	P3TYPE.4	P3TYPE.3	P3TYPE.2	P3TYPE.1	P3TYPE.0
---	---	----------	----------	----------	----------	----------	----------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- 0 = Push-pull Output (Default) / 1 = Open-drain Output

### ✓ P3DIR (F7h) : Port 3 Input/Output Control Register

-	-	P3DIR.5	P3DIR.4	P3DIR.3	P3DIR.2	P3DIR.1	P3DIR.0
---	---	---------	---------	---------	---------	---------	---------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- 0 = Output / 1 = Input (Default)

### ✓ P3SEL (E7h) : Port 3 Pull-up Control Register

-	-	P3SEL.5	P3SEL.4	P3SEL.3	P3SEL.2	P3SEL.1	P3SEL.0
---	---	---------	---------	---------	---------	---------	---------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC\_EN (ADCON[7]) = 1

### ✓ P3 (B0h) : Port 3 Register

-	-	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
---	---	------	------	------	------	------	------

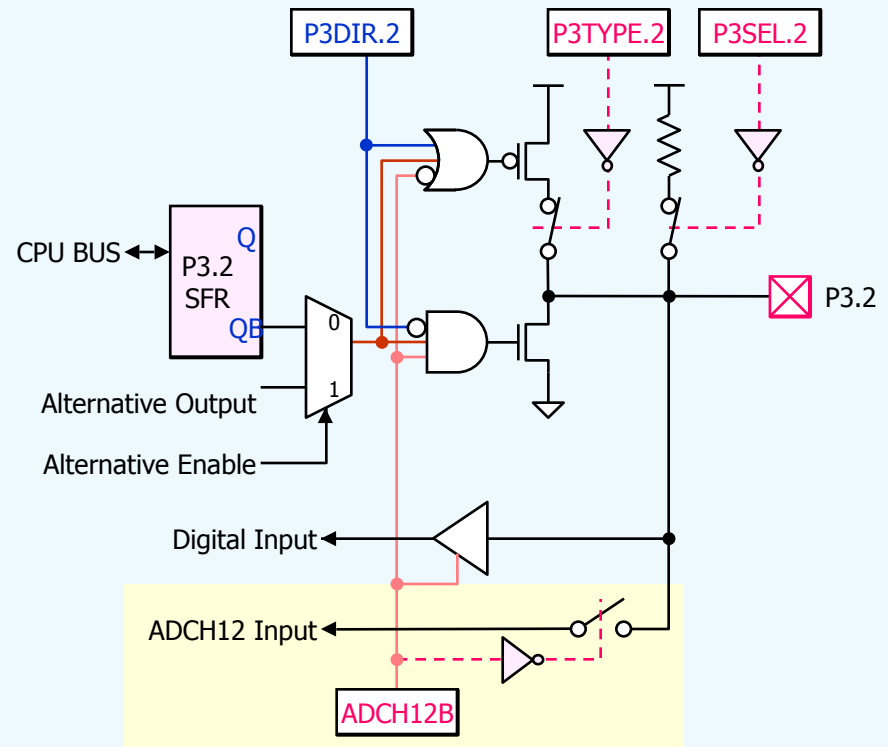
R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

### ✓ ADCHH (DAh) : ADC High Channel Selection High Register

ADCH15B	ADCH14B	ADCH13B	ADCH12B	ADCH11B	ADCH10B	ADCH9B	ADCH8B
---------	---------	---------	---------	---------	---------	--------	--------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ADCHXB = 0 : ADCHX Input Enable (Digital Input Disable).



## 6.6. LVD (Low Voltage Detector)

- ◆ On-chip power-on reset
  - ✓ 2.0V
- ◆ On-chip power-fail interrupt
  - ✓ 2.2V / 2.4V / 2.6V / 2.8V / 3.0V / 3.2V / 3.6V / 4.0V

### ✓ LVDST (97h) : LVD Status Register

LVD7	LVD6	LVD5	LVD4	LVD3	LVD2	LVD1	LVD0
R(0)	R(0)	R(0)	R(0)	R(0)	R(0)	R(0)	R(0)

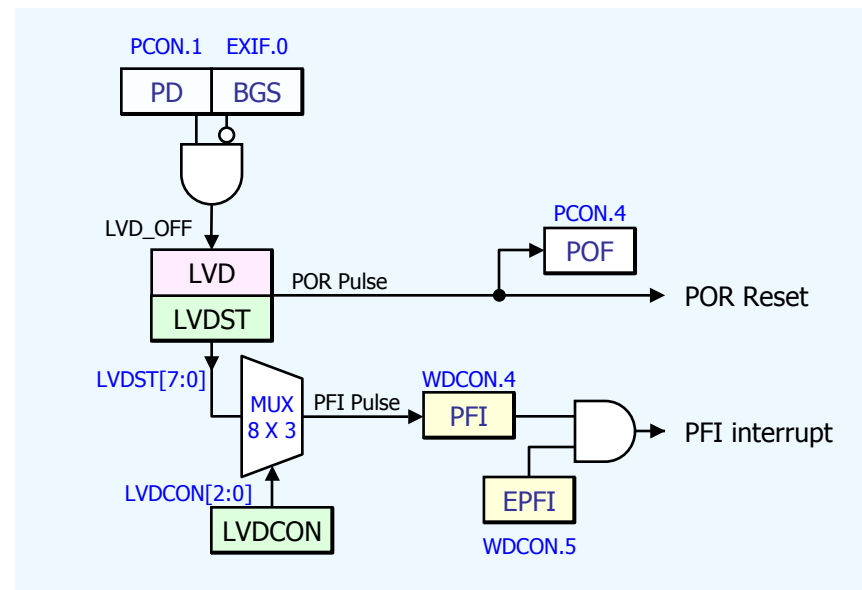
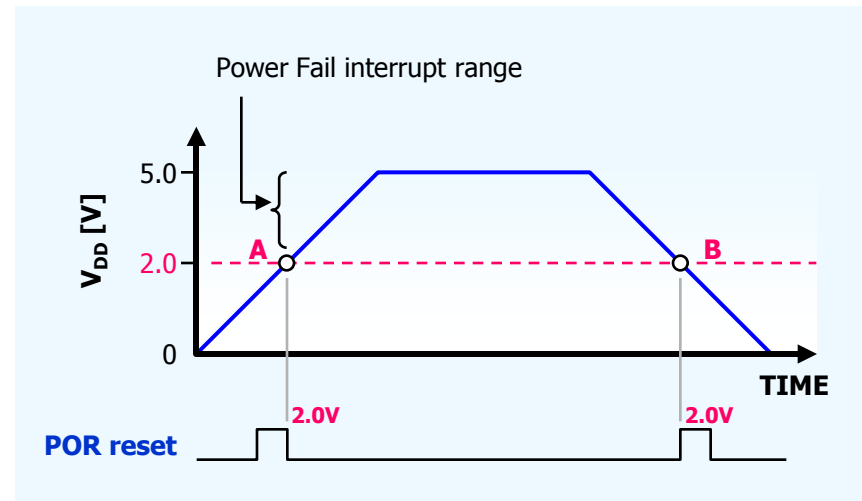
- LVD7 = 1 when VDD ≤ 4.0V.
- LVD6 = 1 when VDD ≤ 3.6V.
- LVD5 = 1 when VDD ≤ 3.2V.
- LVD4 = 1 when VDD ≤ 3.0V.
- LVD3 = 1 when VDD ≤ 2.8V.
- LVD2 = 1 when VDD ≤ 2.6V.
- LVD1 = 1 when VDD ≤ 2.4V.
- LVD0 = 1 when VDD ≤ 2.2V.

### ✓ LVDCON (96h) : LVD Control Register

-	-	-	-	-	LVDCON.2	LVDCON.1	LVDCON.0
					R/W(0)	R/W(0)	R/W(0)

- LVDCON[2:0] : Select the LVD Interrupt Level. (MUX)
- LVDCON[2:0] = 000b, LVD Interrupt Level = 4.0V (Default).
- LVDCON[2:0] = 001b, LVD Interrupt Level = 3.6V.
- LVDCON[2:0] = 010b, LVD Interrupt Level = 3.2V.
- LVDCON[2:0] = 011b, LVD Interrupt Level = 3.0V.
- LVDCON[2:0] = 100b, LVD Interrupt Level = 2.8V.
- LVDCON[2:0] = 101b, LVD Interrupt Level = 2.6V.
- LVDCON[2:0] = 110b, LVD Interrupt Level = 2.4V.
- LVDCON[2:0] = 111b, LVD Interrupt Level = 2.2V.

- ✓ **WDCON** (D8h), **PCON** (87h), and **EXIF** (91h)  
: Refer to Next Slide



## 6.6. LVD (Low Voltage Detector) (Cont'd)

### ✓ **WDCON** (D8h) : Watchdog Timer Control Register

WD1	WD0	EPFI	PFI	WDIF	WTRF	EWT	RWT
-----	-----	------	-----	------	------	-----	-----

R/W(1) R/W(1) R/W(0) R/W(1) R/W(0) R/W(0) R/W(0) R/W(0)

- EPFI : Power-fail interrupt enable.
- PFI : Power-fail interrupt flag.

### ✓ **EXIF** (91h) : External Interrupt Flag Register

-	-	IE3	IE2	XT/RG	RGMD	RGSL	BGS
---	---	-----	-----	-------	------	------	-----

R/W(0) R/W(0) R/W(0) R(1) R/W(0) R/W(1)

- BGS : Band-gap select (Default = 1).

When BGS = 0,  
Band-gap block (LVD) will do not run in power-down mode, but function during normal mode.

When BGS = 1,  
Band-gap block (LVD) will run in power-down mode.

### ✓ **PCON** (87h) : Power Control Register

SMOD1	-	-	POF	GF1	GF0	PD	IDL
-------	---	---	-----	-----	-----	----	-----

R/W(0) R/W(1) R/W(0) R/W(0) R/W(0) R/W(0)

- POF : Power off flag.  
When power-on, this flag bit will be set by H/W.
- PD : Power-down (Stop) mode enable.

## 6.7. WDT (Watchdog Timer)

- ◆ Detect the malfunction of program due to external noise or other causes.
- ◆ Return the operation to the normal condition using WDT interrupt.
- ◆ If enabled, WDT interrupt or WDT reset makes MCU wake up from Stop Mode 2.
- ◆ Watchdog Time-out Values

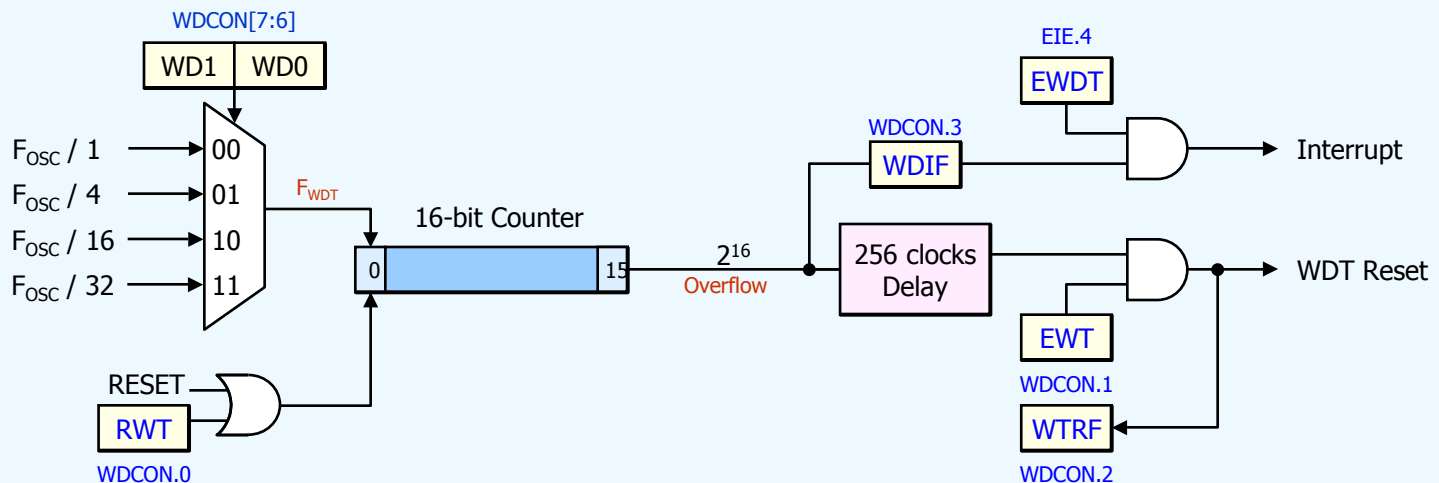
WD1	WD0	Interrupt Time-out (@4MHz)		Reset Time-out (@4MHz)	
0	0	1x2 <sup>16</sup> clocks	16.38 ms	1x2 <sup>16</sup> + 256 clocks	16.45 ms
0	1	4x2 <sup>16</sup> clocks	65.54 ms	4x2 <sup>16</sup> + 256 clocks	65.60 ms
1	0	16x2 <sup>16</sup> clocks	262.14 ms	16x2 <sup>16</sup> + 256 clocks	262.21 ms
1	1	32x2 <sup>16</sup> clocks	524.29 ms	32x2 <sup>16</sup> + 256 clocks	524.35 ms

### ✓ WDCON (D8h) : Watchdog Timer Control Register

WD1	WD0	EPFI	PFI	WDIF	WTRF	EWT	RWT
-----	-----	------	-----	------	------	-----	-----

R/W(1) R/W(1) R/W(0) R/W(1) R/W(0) R/W(0) R/W(0) R/W(0)

- WD[1:0] : WDT Clock Divide(1/4/16/32)
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag. Only cleared by S/W.
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer



\* RWT is only used with WDT mode 0 (WD[1:0] = [0,0]) for MiDAS2.1 Family (Refer to Application Note #009 (AN009))

## 6.8. Timer/Counter : Timer 0/1

- ◆ Compatible with traditional 80C52 Timer/Counter function
- ◆ Time base is 12 clocks.

Mode Timer	Mode 0 (M1,M0=00)	Mode 1 (M1,M0=01)	Mode 2 (M1,M0=10)	Mode 3 (M1,M0=11)
Timer0	13-bit T/C	16-bit T/C	8-bit T/C with automatic reload (TL0 ← TH0)	8-bit T/C (TL0) → Timer0 interrupt 8-bit T/C (TH0) → Timer1 interrupt
Timer1	Not Supported		8-bit T/C with automatic reload (TL1 ← TH1)	Not Supported

### ✓ TMOD (89h) : Timer/Counter 0 Mode Control Register

-	-	-	-	GATE	C/T	M1	M0
---	---	---	---	------	-----	----	----

R/W(0) R/W(0) R/W(0) R/W(0)

- GATE : Timer 0 Gate control. When TR<sub>x</sub> (in TCON) is set and GATE=1, Timer x will run only while INT<sub>x</sub> pin is high (hardware control). When GATE=0, Timer x will run only while TR<sub>x</sub>=1 (software control).
- C/T[2] : Timer 0 Counter/Timer Select.  
0 = Timer by F<sub>OSC</sub>/12. (Default)  
1 = Counter by T0 pin.
- M1, M0 : Timer 0 Mode Select.  
[0,0] : Mode 0. 13-bit T/C.  
[0,1] : Mode 1. 16-bit T/C.  
[1,0] : Mode 2. 8-bit T/C with automatic reload  
[1,1] : Mode 3. Two 8-bit T/C

### ✓ TCON (88h) : Timer/Counter 0/1 Control Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
-----	-----	-----	-----	-----	-----	-----	-----

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- TF1 : Timer 1 Overflow Flag.
- TR1 : Timer 1 Run Enable.
- TF0 : Timer 0 Overflow Flag.
- TR0 : Timer 0 Run Enable.
- IE1 : External Interrupt 1 Flag.
- IT1 : External Interrupt 1 Type Select Flag.  
Edge Detect (IT1=1). Level Detect (IT1=0).
- IE0 : External Interrupt 0 Flag.
- IT0 : External Interrupt 0 Type Select Flag.  
Edge Detect (IT0=1). Level Detect (IT0=0).

### ✓ TLO (8Ah) : Timer/Counter 0 Low Byte Register

TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

### ✓ TH0 (8Ch) : Timer/Counter 0 High Byte Register

TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

### ✓ TL1 (8Bh) : Timer/Counter 1 Low Byte Register

TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
-------	-------	-------	-------	-------	-------	-------	-------

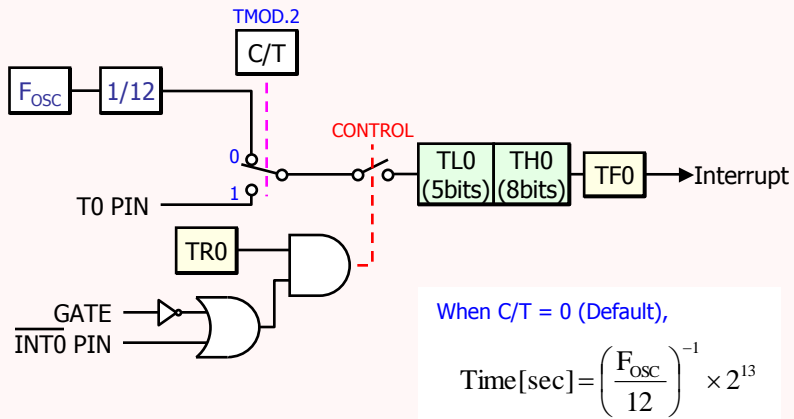
R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

### ✓ TH1 (8Dh) : Timer/Counter 1 High Byte Register

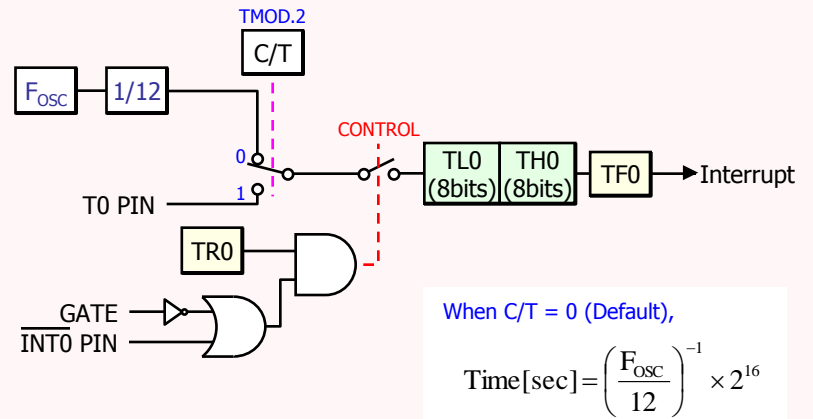
TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

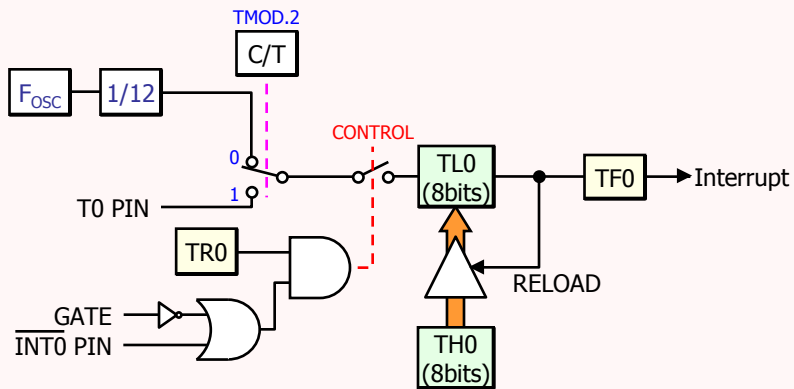
# 6.8. Timer/Counter : Timer 0 Mode Description



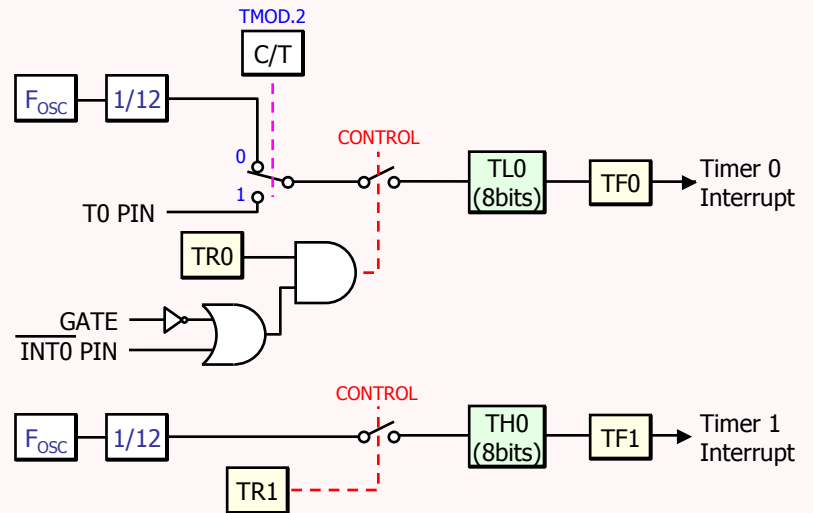
**[Mode 0]**



**[Mode 1]**

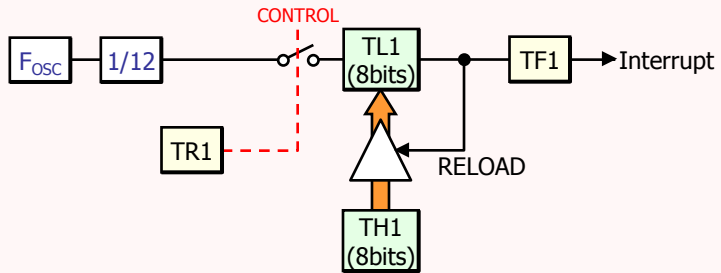


**[Mode 2]**



**[Mode 3]**

## 6.8. Timer/Counter : Timer 1 Mode Description



[Mode 2]

# 6.9. UART

◆ Simplified 8052 UART  
( only UART Mode 1 is supported.)

	Data Size		Baudrate
	Mode 1	10 bits	Start bit(0) 8 data bit Stop bit(1)

◆ UART Mode 1  
(Using Timer 1 Overflow)

$$\text{Baudrate} = \frac{2^{\text{SMOD1}}}{32} \times F_{\text{osc}} \times \frac{1}{12 \times [256 - (\text{TH1})]}$$

[Baudrate Examples]

Baudrate	UART Mode	F <sub>osc</sub> [MHz]	SMOD1	Timer 1		
				C/T	Mode	Reload Value (TH1)
62.5 KHz	Mode 1	12	1	0	Mode 2 8-bit Auto-reload	FFh
19.2 KHz		11.0592	1	0		FDh
9.6 KHz		11.0592	0	0		FDh
4.8 KHz		11.0592	0	0		FAh
2.4 KHz		11.0592	0	0		F4h
1.2 KHz		11.0592	0	0		E8h
137.5 Hz		11.0592	0	0		1Dh
110 Hz		6	0	0		72h

✓ **PCON** (87h) : Power Control Register

SMOD1	-	-	POF	GF1	GF0	PD	IDL
R/W(0)			R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SMOD1 : Timer 1 baudrate double in UART mode.

✓ **SCON** (98h) : Serial Port Control Register

-	-	-	REN	-	-	TI	RI
			R/W(0)			R/W(0)	R/W(0)

- REN : Serial Reception Enable.  
If user want to receive the data with UART, the REN flag bit is set to 1.
- TI : Transmission Interrupt Flag. Must be cleared by S/W.
- RI : Reception Interrupt Flag. Must be cleared by S/W.

✓ **SBUF** (99h) : Serial Data Buffer Register

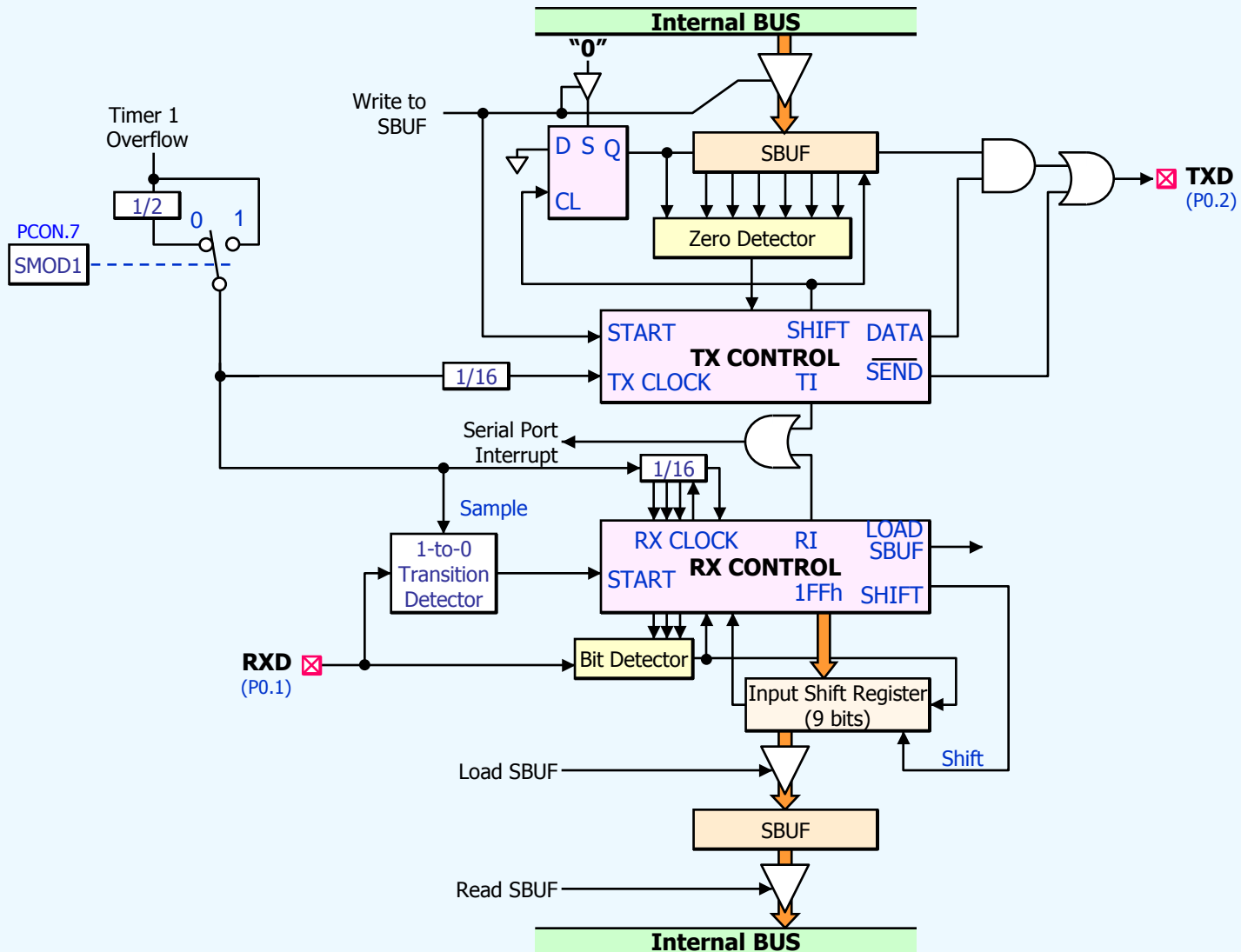
SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Transmission buffer and reception buffer are separated.
- Read and Write address are same.

✓ **TH1** (8Dh) : Timer/Counter 1 High Byte Register

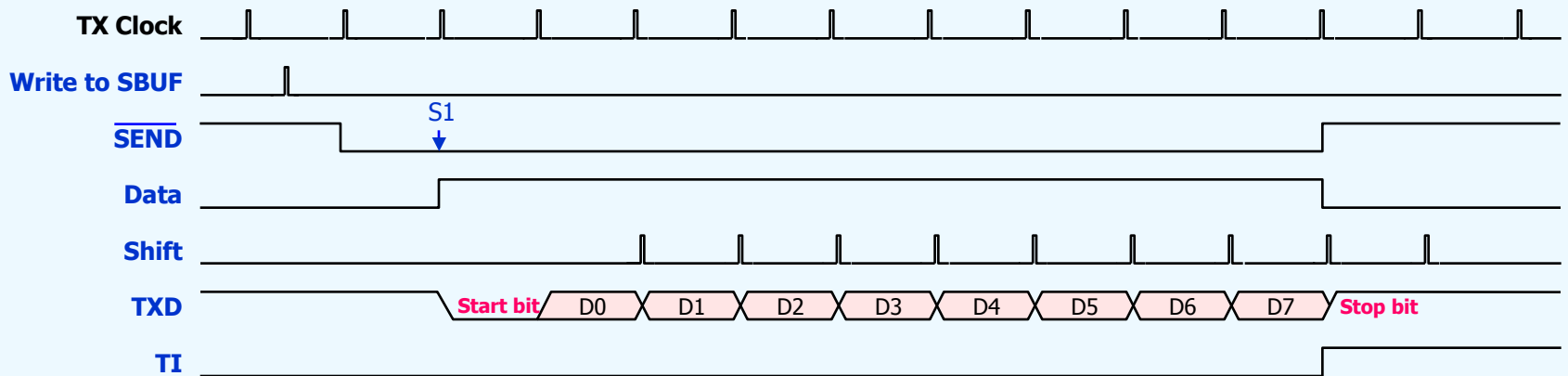
TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

# 6.9. UART : Mode 1 Function

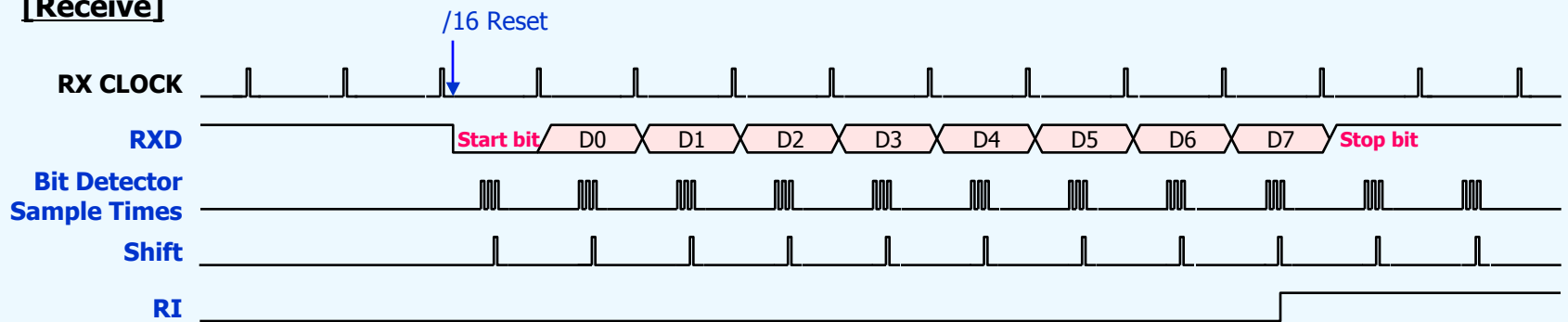


## 6.9. UART : Mode 1 Timing

### [Transmit]

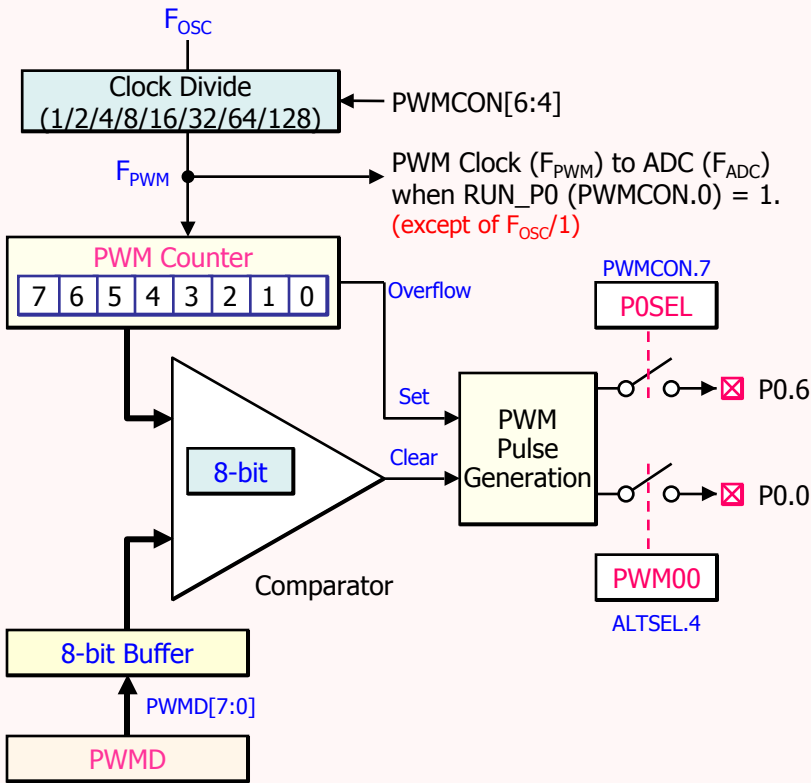


### [Receive]



# 6.10. PWM (Pulse Width Modulator)

- ◆ Intelligent 1-channel 8-bit PWM
- ◆ PWM Data buffer Update (8-bit Overflow Update)
- ◆ PWM Counter can be cleared by S/W.
- ◆ PWM is stopped or started (resumed) by S/W.



## ✓ PWMCON (DCh) : PWM Control Register

POSEL	PS2_P0	PS1_P0	PS0_P0	-	PWMF	CLR_P0	RUN_P0
R/W(0)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)

- POSEL : PWM Waveform Output Enable to P0.6.
- PS2\_P0, PS1\_P0, PS0\_P0 : Pre-scaled Clock Selection.  
 $[0,0,0] = F_{OSC}/1$ ,  $[0,0,1] = F_{OSC}/2$ ,  $[0,1,0] = F_{OSC}/4$ ,  
 $[0,1,1] = F_{OSC}/8$ ,  $[1,0,0] = F_{OSC}/16$ ,  $[1,0,1] = F_{OSC}/32$ ,  
 $[1,1,0] = F_{OSC}/64$ ,  $[1,1,1] = F_{OSC}/128$   
*\* PWM Clock ( $F_{PWM}$ ) to ADC should not be set to  $F_{OSC}/1$ .*
- PWMF : PWM Interrupt Flag. Cleared by S/W.
- CLR\_P0 : Counter Reset Enable. Cleared by H/W.
- RUN\_P0 : Counter Start Enable. PWM Clock ( $F_{PWM}$ ) Output Enable.

## ✓ PWMD (DEh) : PWM Duty Data Register

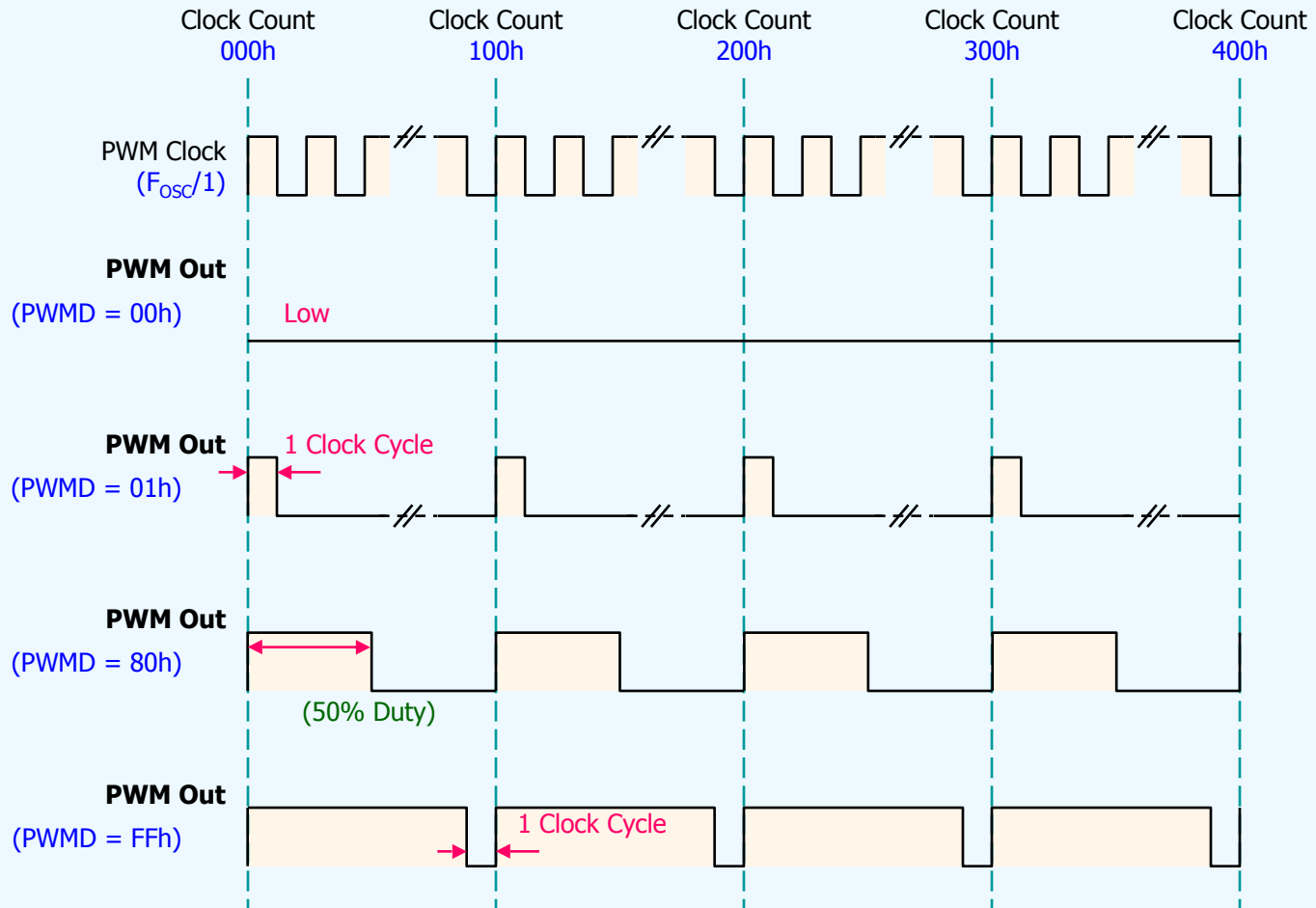
PWMD.7	PWMD.6	PWMD.5	PWMD.4	PWMD.3	PWMD.2	PWMD.1	PWMD.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

## ✓ ALTSEL (E3h) : Alternative Function Control Register

IOXEN	IORSTEN	CLO	PWM00	TV0	TX	-	-
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)		

- PWM00 : PWM Waveform Output Enable to P0.0.

## 6.10. PWM : Pulse Generation



# 6.11. ADC (Analog-to-Digital Converter)

- ◆ 28-channel 10-bit ADC (SAR Type)
- ◆ Max. 104ksps(samples per sec.) @  $F_{ADC} = 10\text{MHz} \ \& \ 5\text{V}$ . (Max. 52ksps @  $F_{ADC} = 5\text{MHz} \ \& \ 3\text{V}$ )

## ✓ ADCSELH (E1h) : ADC Channel Selection High Register

ADC11B	ADC10B	ADC9B	ADC8B	ADC7B	ADC6B	ADC5B	ADC4B
--------	--------	-------	-------	-------	-------	-------	-------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- $ADCXB = 0$  : ADCX Input Enable (Digital Input Disable).

## ✓ ADCSEL (E2h) : ADC Channel Selection Low & MUX Selection Reg.

ADC3B	ADC2B	ADC1B	ADC0B	CH3	CH2	CH1	CH0
-------	-------	-------	-------	-----	-----	-----	-----

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- $ADCXB = 0$  : ADCX Input Enable (Digital Input Disable).

- CH[3:0] : ADC MUX Selection.
  - 0000b = ADC0 Selection (0h)
  - 0001b = ADC1 Selection (1h)
  - 0010b = ADC2 Selection (2h)
  - 0011b = ADC3 Selection (3h)
  - 0100b = ADC4 Selection (4h)
  - 0101b = ADC5 Selection (5h)
  - 0110b = ADC6 Selection (6h)
  - 0111b = ADC7 Selection (7h)
  - 1000b = ADC8 Selection (8h)
  - 1001b = ADC9 Selection (9h)
  - 1010b = ADC10 Selection (Ah)
  - 1011b = ADC11 Selection (Bh)
  - 1100b = No ADC input select (Ch)
  - 1101b = No ADC input select (Dh)
  - 1110b = No ADC input select (Eh)
  - 1111b = No ADC input select (Fh, Default)

## ✓ ADCHH (DAh) : ADC High Channel High Enable Register

ADCH15B	ADCH14B	ADCH13B	ADCH12B	ADCH11B	ADCH10B	ADCH9B	ADCH8B
---------	---------	---------	---------	---------	---------	--------	--------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- $ADCHXB = 0$  : ADCHX Input Enable (Digital Input Disable).

## ✓ ADCHL (D9h) : ADC High Channel Selection Low Register

ADCH7B	ADCH6B	ADCH5B	ADCH4B	ADCH3B	ADCH2B	ADCH1B	ADCH0B
--------	--------	--------	--------	--------	--------	--------	--------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- $ADCHXB = 0$  : ADCHX Input Enable (Digital Input Disable).

## ✓ ADCHSEL (DBh) : ADC High Channel Selection Register

CH_SEL	-	-	-	CHH3	CHH2	CHH1	CHH0
--------	---	---	---	------	------	------	------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- CH\_SEL : ADC MUX Selector with CHH[3:0] & CH[3:0].
  - 0 = CH[3:0] → ADC[11:0] Enable / ADCH[15:0] Disable (Default)
  - 1 = CHH[3:0] → ADC[11:0] Disable/ ADCH[15:0] Enable
- CHH[3:0] : ADC MUX Selection for High Channel
  - 0000b = ADCH0 Selection (0h)
  - 0001b = ADCH1 Selection (1h)
  - 0010b = ADCH2 Selection (2h)
  - 0011b = ADCH3 Selection (3h)
  - 0100b = ADCH4 Selection (4h)
  - 0101b = ADCH5 Selection (5h)
  - 0110b = ADCH6 Selection (6h)
  - 0111b = ADCH7 Selection (7h)
  - 1000b = ADCH8 Selection (8h)
  - 1001b = ADCH9 Selection (9h)
  - 1010b = ADCH10 Selection (Ah)
  - 1011b = ADCH11 Selection (Bh)
  - 1100b = ADCH12 Selection (Ch)
  - 1101b = ADCH13 Selection (Dh)
  - 1110b = ADCH14 Selection (Eh)
  - 1111b = ADCH15 Selection (Fh)

## 6.11. ADC (Analog-to-Digital Converter) (Cont'd)

✓ **ADCON** (EFh) : ADC Control & ADC Result Low Register : SAR[1:0]

AD_EN	AD_REQ	AD_END	ADCF	-	ADIV	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)		R/W(0)	R/W(0)	R/W(0)

- AD\_EN : AD Conversion Enable.
- AD\_REQ : AD Conversion Request.  
Cleared by H/W when AD\_END goes to 1 from 0.
- AD\_END : Current ADC Status.  
0 = ADC is running now.  
User must check the ADCF instead of AD\_END.
- ADCF : ADC Interrupt Flag.  
Must be cleared by S/W.
- ADIV : ADC Input Clock ( $F_{ADC}$ ) Select.  
0 = System Clock ( $F_{OSC}$ ) / 2. (Default)  
1 = PWM Input Clock ( $F_{PWM}$ )  
PWM Clock for ADC should not be set to  $F_{OSC}/1$ .
- SAR[1:0] : Low Bits of ADC Result Value. (Total 10 bits)

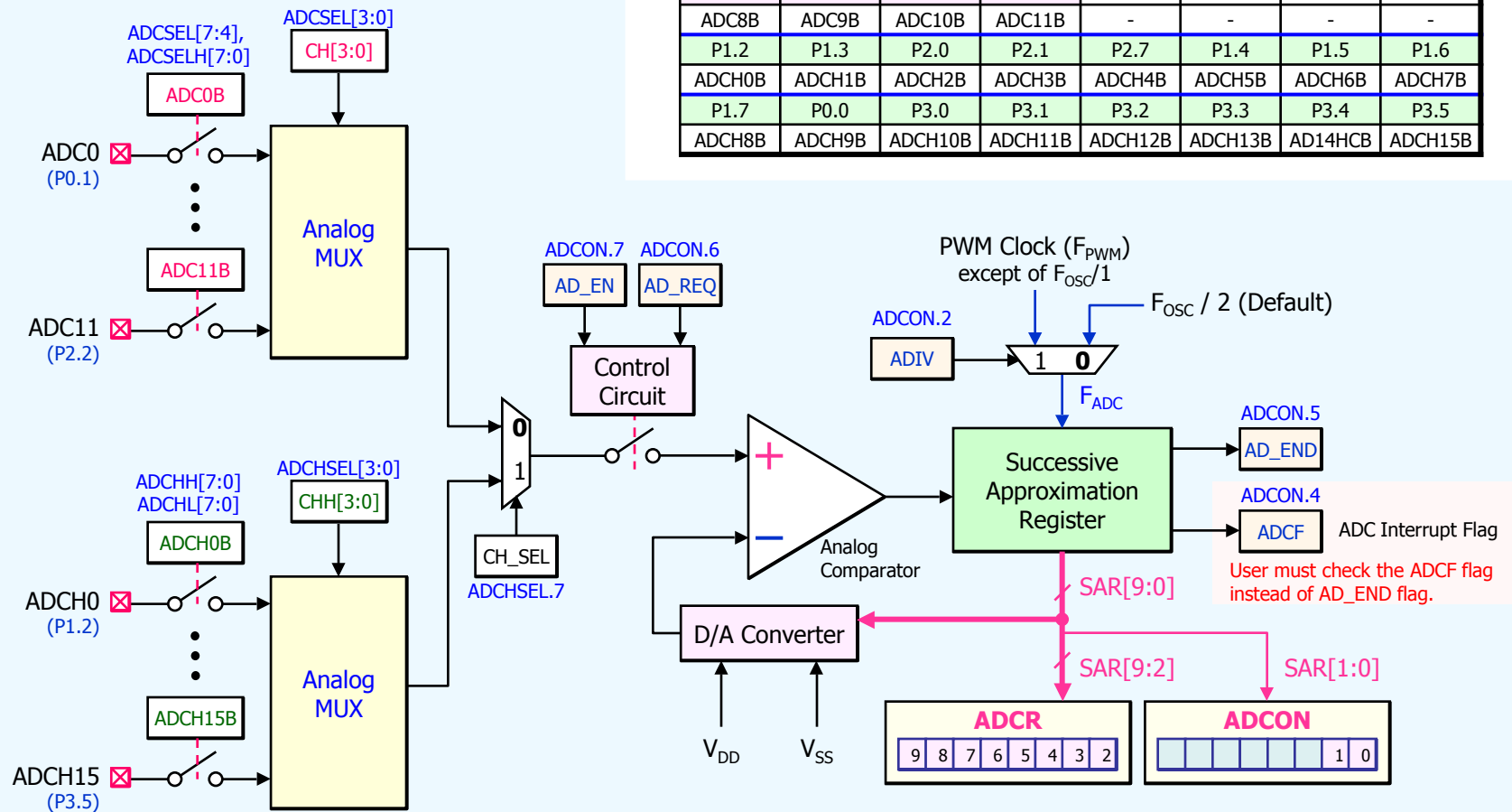
✓ **ADCR** (EEh) : ADC Result High Register

SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

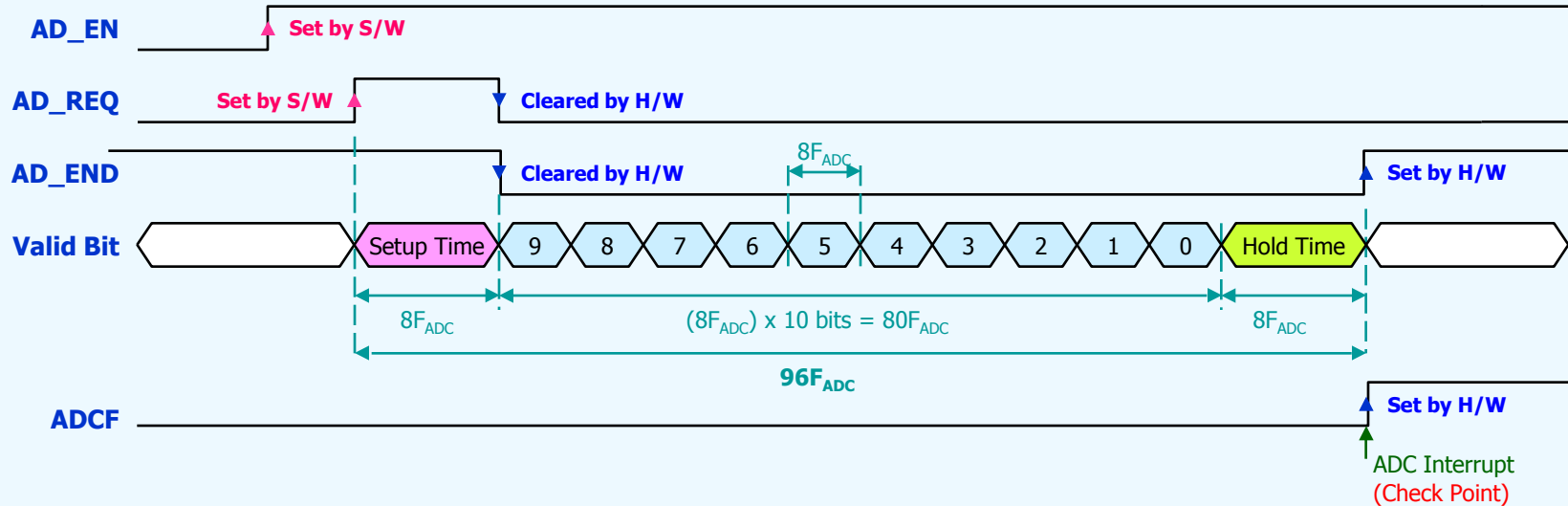
# 6.11. ADC (Analog-to-Digital Converter)

[ ADC Input Channel Selectors versus Port Pins ]

P0.1	P0.2	P0.3	P0.4	P0.5	P0.6	P0.7	P2.6
ADC0B	ADC1B	ADC2B	ADC3B	ADC4B	ADC5B	ADC6B	ADC7B
P2.5	P2.4	P2.3	P2.2	-	-	-	-
ADC8B	ADC9B	ADC10B	ADC11B	-	-	-	-
P1.2	P1.3	P2.0	P2.1	P2.7	P1.4	P1.5	P1.6
ADCH0B	ADCH1B	ADCH2B	ADCH3B	ADCH4B	ADCH5B	ADCH6B	ADCH7B
P1.7	P0.0	P3.0	P3.1	P3.2	P3.3	P3.4	P3.5
ADCH8B	ADCH9B	ADCH10B	ADCH11B	ADCH12B	ADCH13B	AD14HCB	ADCH15B



## 6.11. ADC : Conversion Timing



- ✓ **AD\_EN** : AD Conversion Enable Signal.  
Set or Cleared by S/W.
- ✓ **AD\_REQ** : AD Conversion Request Bit.  
Set by S/W and Cleared by H/W.  
This bit must be set at each sample conversion.
- ✓ **AD\_END** : Set or Cleared by H/W.  
Clear when Conversion started.  
Set when Conversion ended.
- ✓ **ADCF** : AD Conversion Interrupt Flag.  
Set by H/W and Cleared by S/W.  
A User should clear ADCF bit in ADC interrupt routine.  
A User must check the ADCF flag instead of AD\_END.

[An Example of ADC Conversion Table]

System Clock ( $F_{OSC}$ )	Divide (ADIV=0)	$F_{ADC}$	$T_{ADC}$ ( $1/F_{ADC}$ )	1 Sample Conversion Time
20MHz @ 5V	$F_{OSC}/2$	10MHz	100ns	9.6us
10MHz @ 5V	$F_{OSC}/2$	5MHz	200ns	19.2us
10MHz @ 3V	$F_{OSC}/2$	5MHz	200ns	19.2us
5MHz @ 3V	$F_{OSC}/2$	2.5MHz	400ns	38.4us

## 6.12. I<sup>2</sup>C Master / Slave

- ◆ Master : Max. 300kHz (@12MHz<sub>oscr</sub>, 3.3V<sub>dd</sub>)
- ◆ Slave : 74 ~ 317kHz (@12MHz<sub>oscr</sub>, 3.3V<sub>dd</sub>)
- ◆ 7-bit Addressing Mode
- ◆ Single Byte / Multi Bytes Supported

### ✓ I2C\_SC0N (9Ah) : I<sup>2</sup>C Slave Control Register

-	WR	RD	BUSY	-	I2C_SIF	MODE	RUN
R(0)	R(0)	R(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- WR : I<sup>2</sup>C Write Operation Status. Cleared by H/W.
- RD : I<sup>2</sup>C Read Operation Status. Cleared by H/W.
- BUSY : Current I<sup>2</sup>C Slave Status. Cleared by H/W.  
If BUSY = 1, I<sup>2</sup>C slave is running now.
- I2C\_SIF : I<sup>2</sup>C Slave Interrupt Flag.  
It is set each time a byte is received or transmitted.  
Cleared by S/W.
- MODE : I<sup>2</sup>C Slave Mode.  
0 = Mode 0. Including Memory Address (Default).  
1 = Mode 1, No Memory Address.
- RUN : I<sup>2</sup>C Slave Start.  
Cleared by S/W.

### ✓ I2C\_SDEV (9Bh) : I<sup>2</sup>C Slave Device Address Register

SDEV.7	SDEV.6	SDEV.5	SDEV.4	SDEV.3	SDEV.2	SDEV.1	SDEV.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SDEV[7:1] : I<sup>2</sup>C Slave Device Address.
- SDEV[0] : Not Used. Don't Care.

### ✓ I2C\_SADR (9Ch) : I<sup>2</sup>C Slave Memory Address Register

SADR.7	SADR.6	SADR.5	SADR.4	SADR.3	SADR.2	SADR.1	SADR.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

### ✓ I2C\_SDAT (9Dh) : I<sup>2</sup>C Slave Data Register

SDAT.7	SDAT.6	SDAT.5	SDAT.4	SDAT.3	SDAT.2	SDAT.1	SDAT.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

## 6.12. I<sup>2</sup>C Master / Slave (Cont'd)

### ✓ I2C\_MDAT (9Eh) : I<sup>2</sup>C Master Data Register

MDAT.7	MDAT.6	MDAT.5	MDAT.4	MDAT.3	MDAT.2	MDAT.1	MDAT.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

### ✓ I2C\_MCON (A2h) : I<sup>2</sup>C Master Control Register

-	-	-	I2C_MIF	OP	BYPASS	MODE	RUN
			R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- I2C\_MIF : I<sup>2</sup>C Master Interrupt Flag.  
It is set each time a byte is received or transmitted.  
Cleared by S/W.
- OP : I<sup>2</sup>C Read/Write Operation.  
0 = Write Operation (Default).  
1 = Read Operation.
- BYPASS : Bypass Mode in I<sup>2</sup>C Master and Slave.
- MODE : I<sup>2</sup>C Master Mode.  
0 = Mode 0. Including Memory Address (Default).  
1 = Mode 1. No Memory Address.
- RUN : I<sup>2</sup>C Master Start.  
Cleared by H/W.

### ✓ I2C\_MDEV (A3h) : I<sup>2</sup>C Maser Device Address Register

MDEV.7	MDEV.6	MDEV.5	MDEV.4	MDEV.3	MDEV.2	MDEV.1	MDEV.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- MDEV[7:1] : I<sup>2</sup>C Master Device Address.
- MDEV[0] : Not Used. Don't Care.

### ✓ I2C\_MADR (A4h) : I<sup>2</sup>C Maser Memory Address Register

MADR.7	MADR.6	MADR.5	MADR.4	MADR.3	MADR.2	MADR.1	MADR.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

### ✓ I2C\_MNUM (A5h) : I<sup>2</sup>C Master Multi-byte Number Register

MNUM.7	MNUM.6	MNUM.5	MNUM.4	MNUM.3	MNUM.2	MNUM.1	MNUM.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Number of Multi-byte = I2C\_MNUM + 1.

### ✓ I2C\_MSCL (A6h) : I<sup>2</sup>C Master Clock Scale Factor Low Byte Register

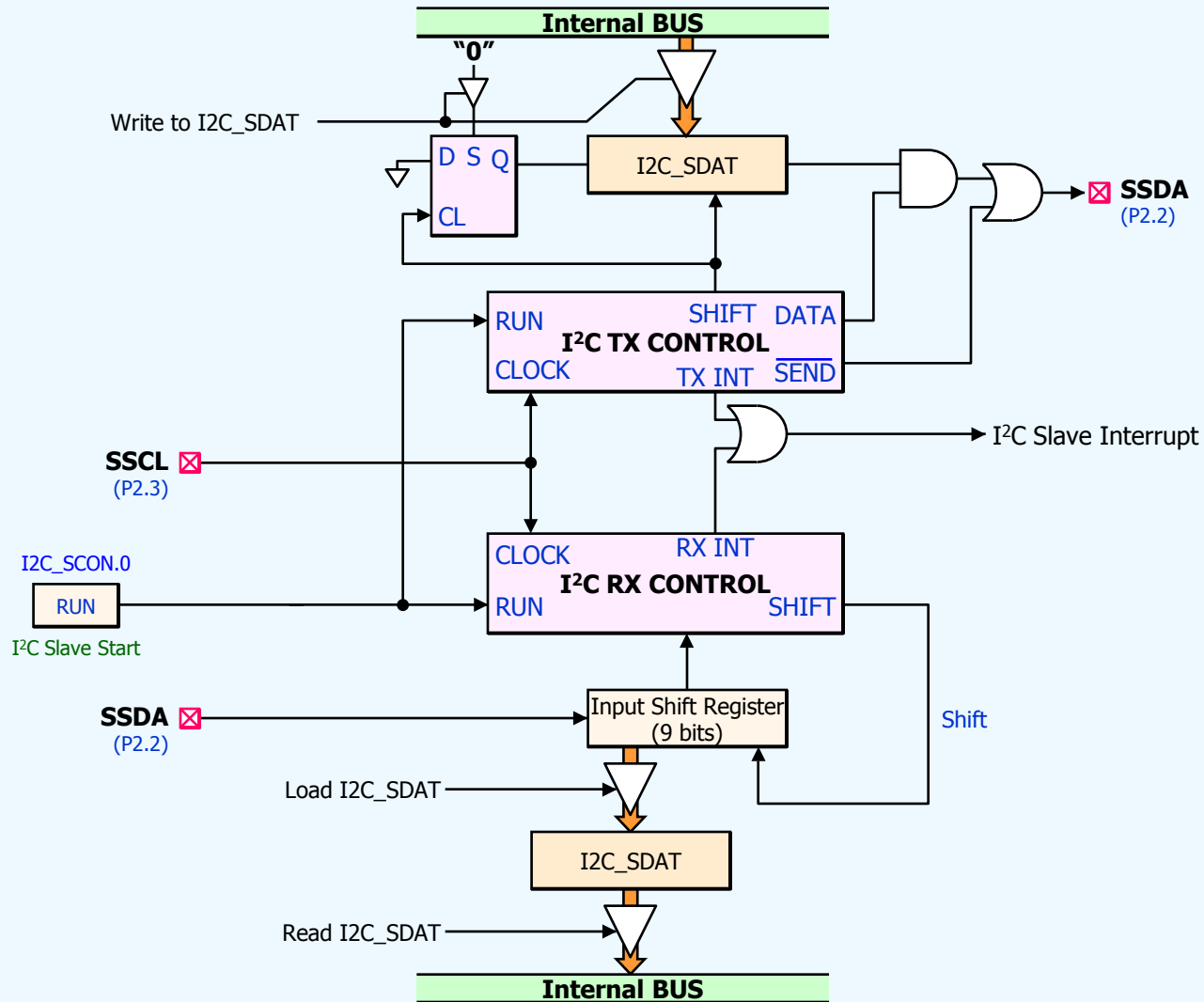
MSCL.7	MSCL.6	MSCL.5	MSCL.4	MSCL.3	MSCL.2	MSCL.1	MSCL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Frequency of I<sup>2</sup>C Master ( $F_{I2C}$ ) =  $F_{Osc} / \{(I2C_MSCH, I2C_MSCL+1)*4\}$ .

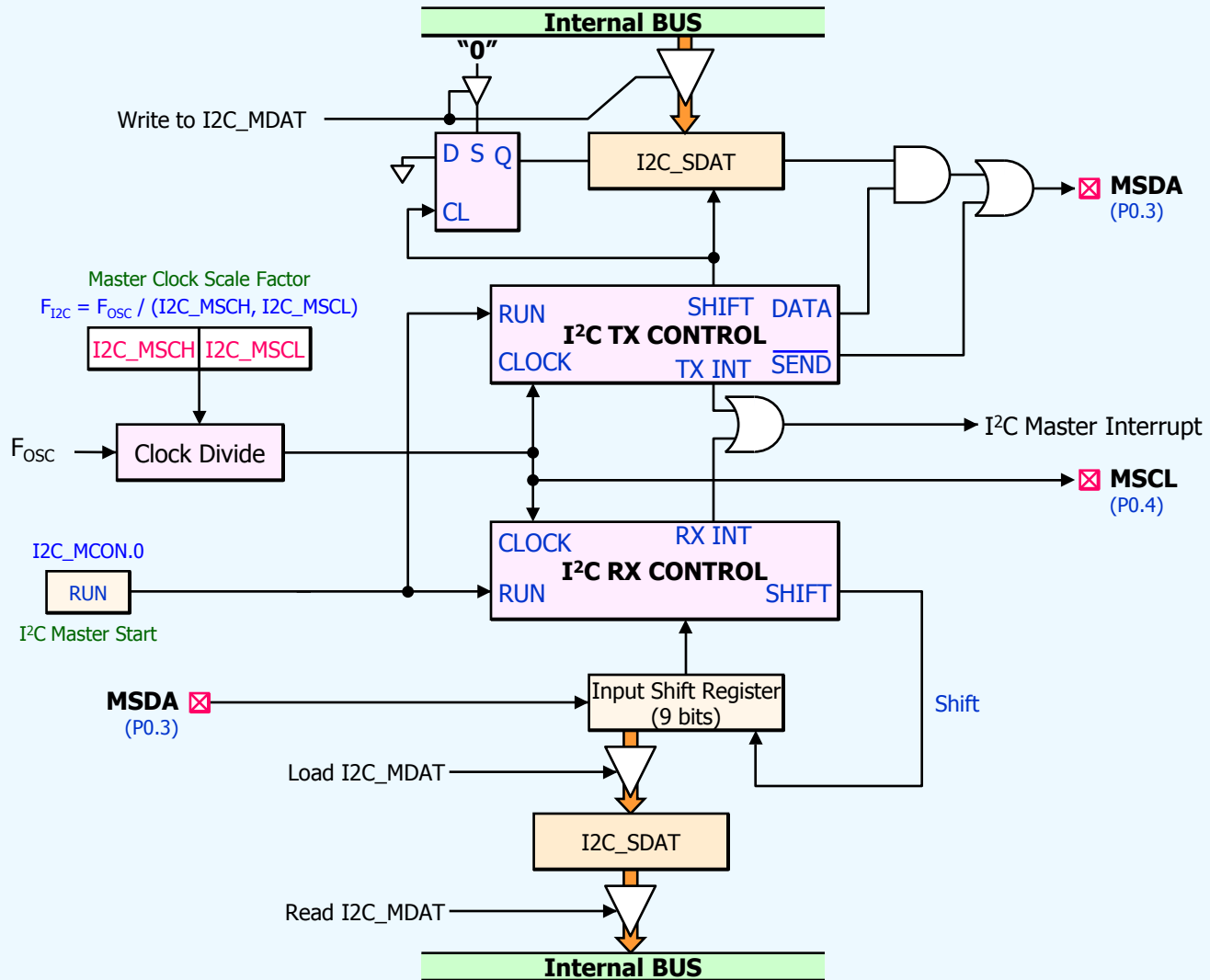
### ✓ I2C\_MSCH (A7h) : I<sup>2</sup>C Master Clock Scale Factor High Byte Register

MSCH.7	MSCH.6	MSCH.5	MSCH.4	MSCH.3	MSCH.2	MSCH.1	MSCH.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

## 6.12. I<sup>2</sup>C : Slave Function



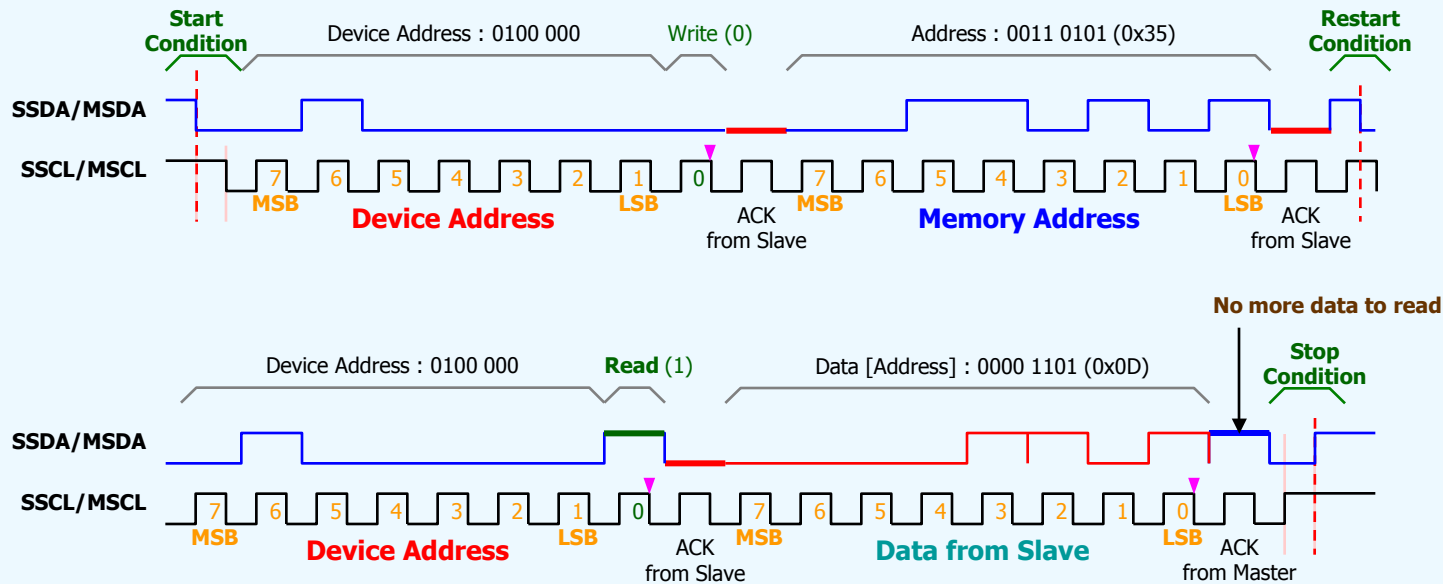
# 6.12. I<sup>2</sup>C : Master Function



## 6.12. I<sup>2</sup>C : Slave & Master Timing (1/7)

### ◆ 1 Byte Read Timing with Memory Address

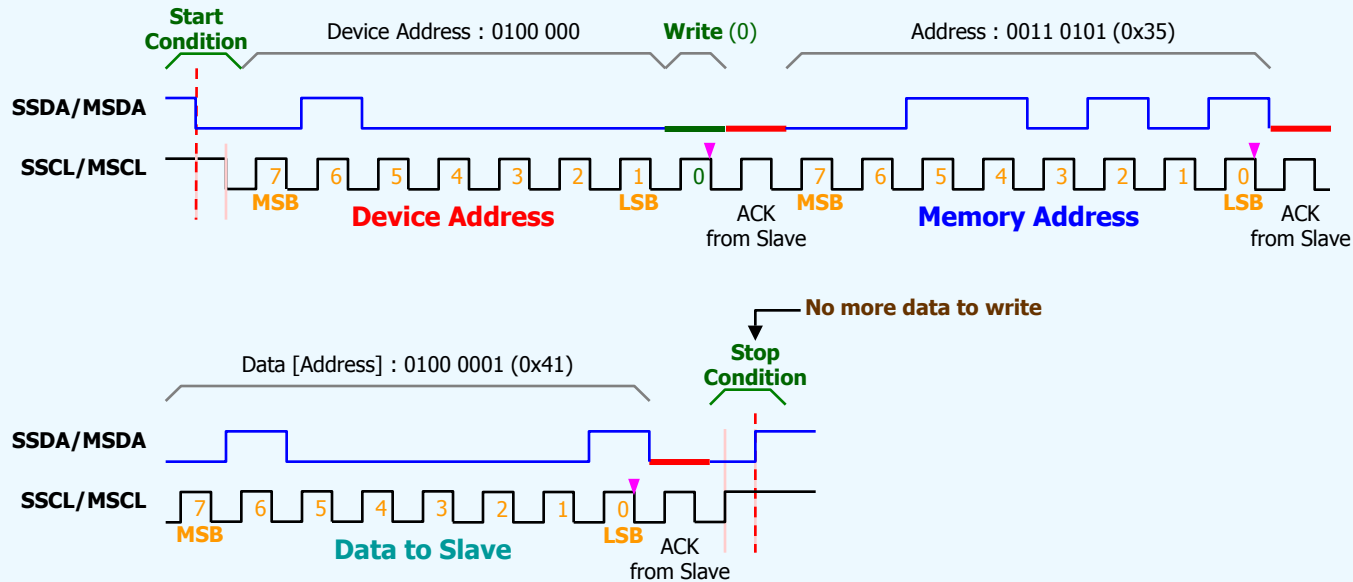
- ✓ I2C\_SCON.1 (MODE) / I2C\_MCON.1 (MODE) = 0 (Mode 0, Including Memory Address; Default).



## 6.12. I<sup>2</sup>C : Slave & Master Timing (2/7)

### ◆ 1 Byte Write Timing with Memory Address

- ✓ I2C\_SCON.1 (MODE) / I2C\_MCON.1 (MODE) = 0 (Mode 0, Including Memory Address; Default).

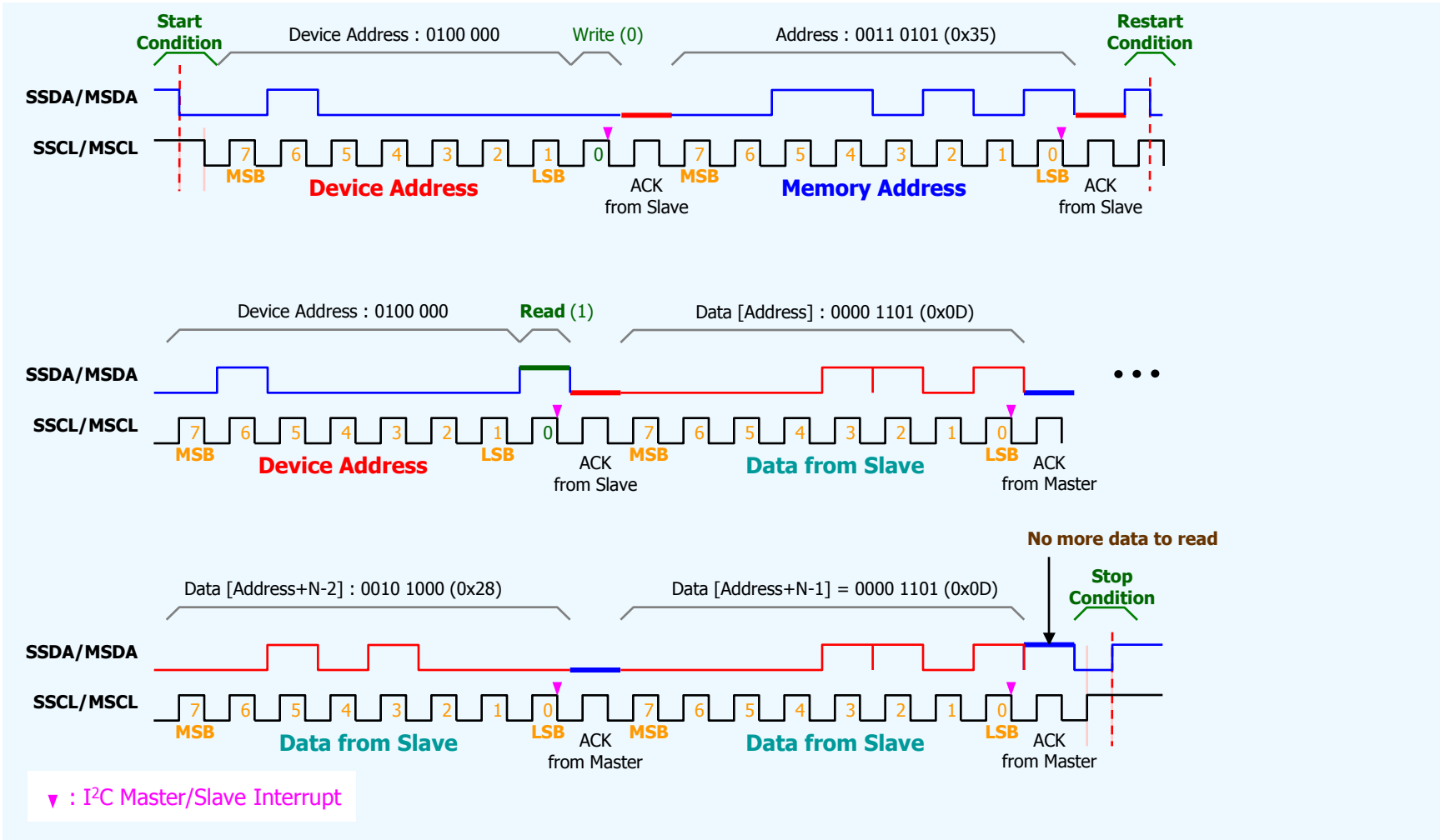


▼ : I<sup>2</sup>C Master/Slave Interrupt

## 6.12. I<sup>2</sup>C : Slave & Master Timing (3/7)

### ◆ Multi (N) Bytes Read Timing with Memory Address

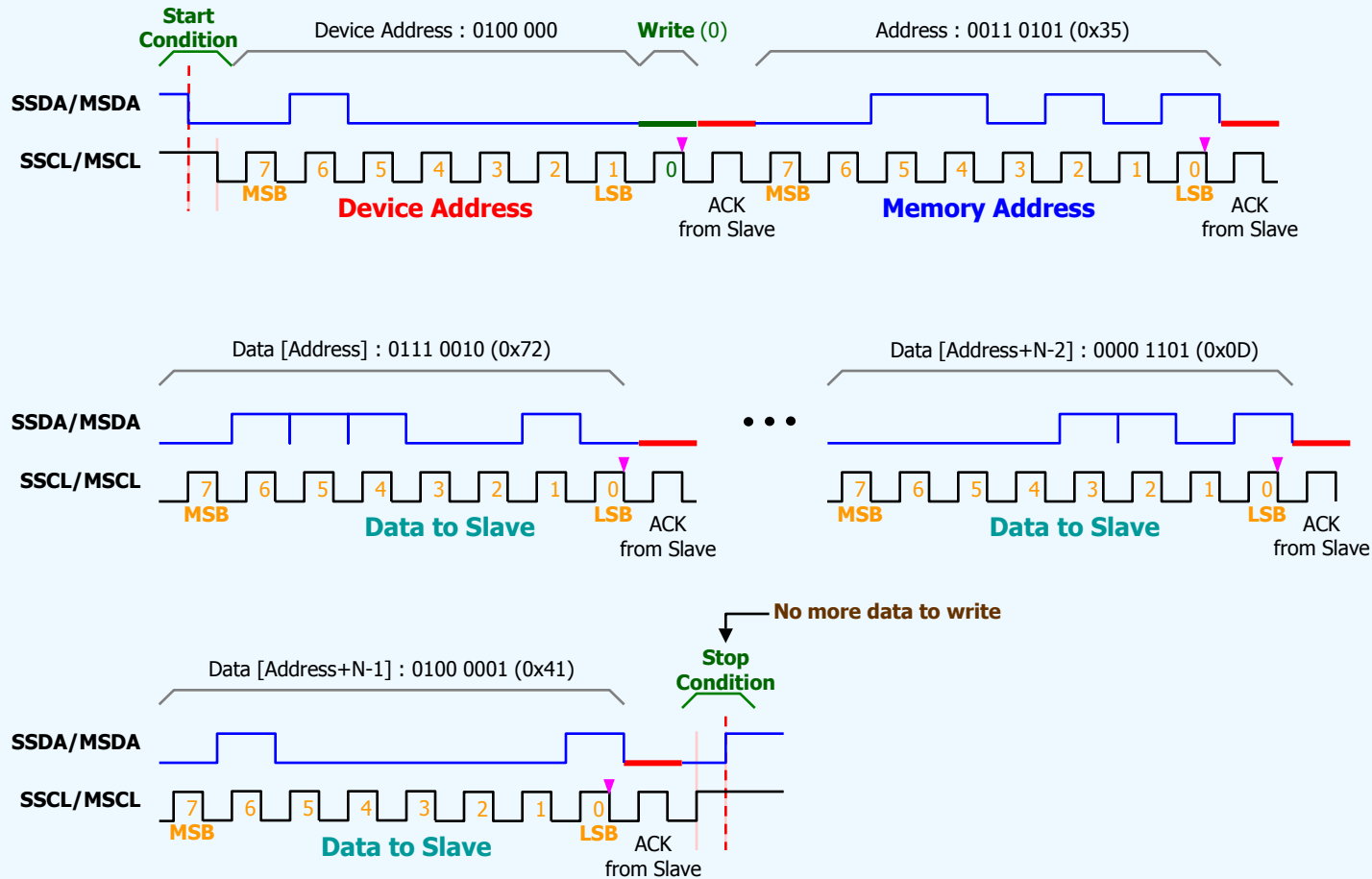
- ✓ I2C\_SCON.1 (MODE) / I2C\_MCON.1 (MODE) = 0 (Mode 0, Including Memory Address; Default).



# 6.12. I<sup>2</sup>C : Slave & Master Timing (4/7)

## ◆ Multi (N) Bytes Write Timing with Memory Address

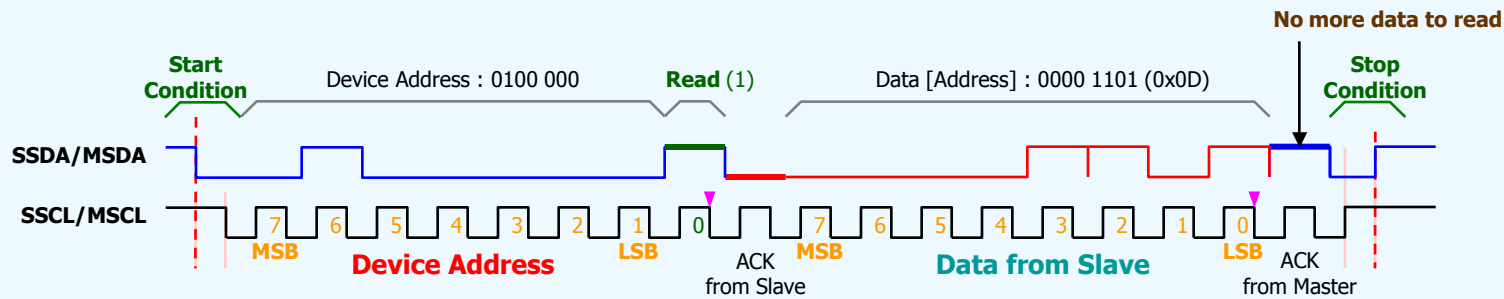
- ✓ I2C\_SCON.1 (MODE) / I2C\_MCON.1 (MODE) = 0 (Mode 0, Including Memory Address; Default).



## 6.12. I<sup>2</sup>C : Slave & Master Timing (5/7)

### ◆ 1 Byte Read Timing without Memory Address

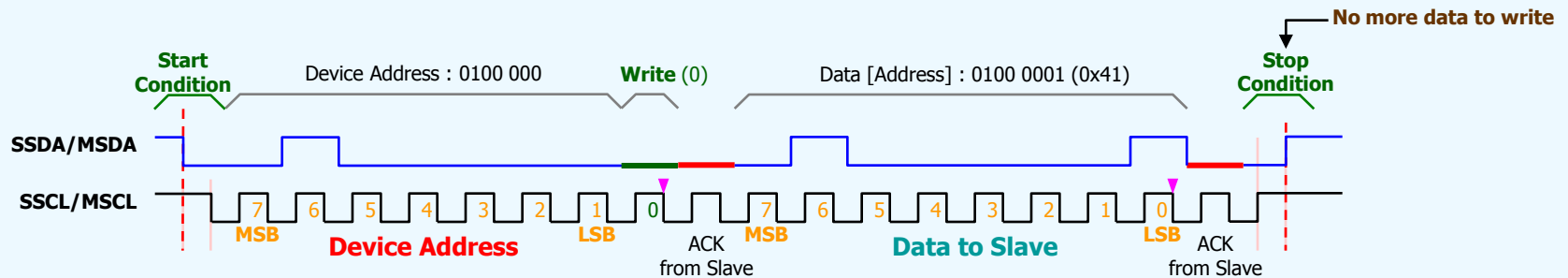
- ✓ I2C\_SCON.1 (MODE) / I2C\_MCON.1 (MODE) = 1 (Mode 1, No Memory Address).



▼ : I<sup>2</sup>C Master/Slave Interrupt

### ◆ 1 Byte Write Timing without Memory Address

- ✓ I2C\_SCON.1 (MODE) / I2C\_MCON.1 (MODE) = 1 (Mode 1, No Memory Address).

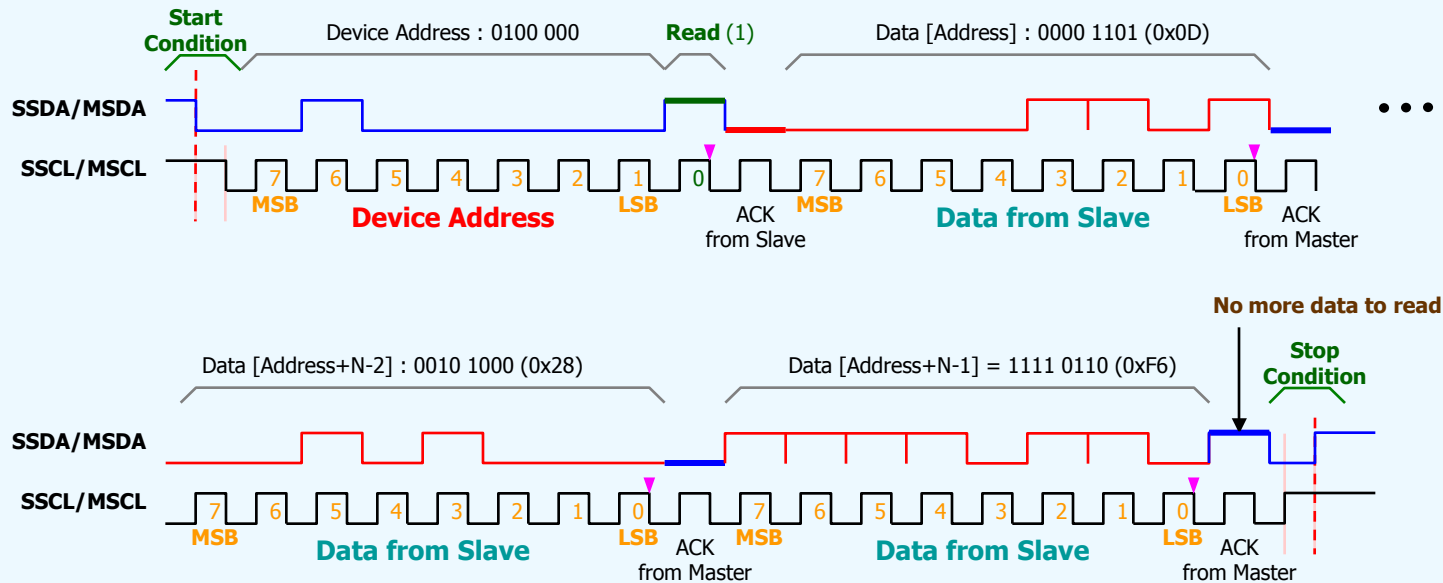


▼ : I<sup>2</sup>C Master/Slave Interrupt

## 6.12. I<sup>2</sup>C : Slave & Master Timing (6/7)

### ◆ Multi (N) Bytes Read Timing without Memory Address

- ✓ I2C\_SCON.1 (MODE) / I2C\_MCON.1 (MODE) = 1 (Mode 1, No Memory Address).

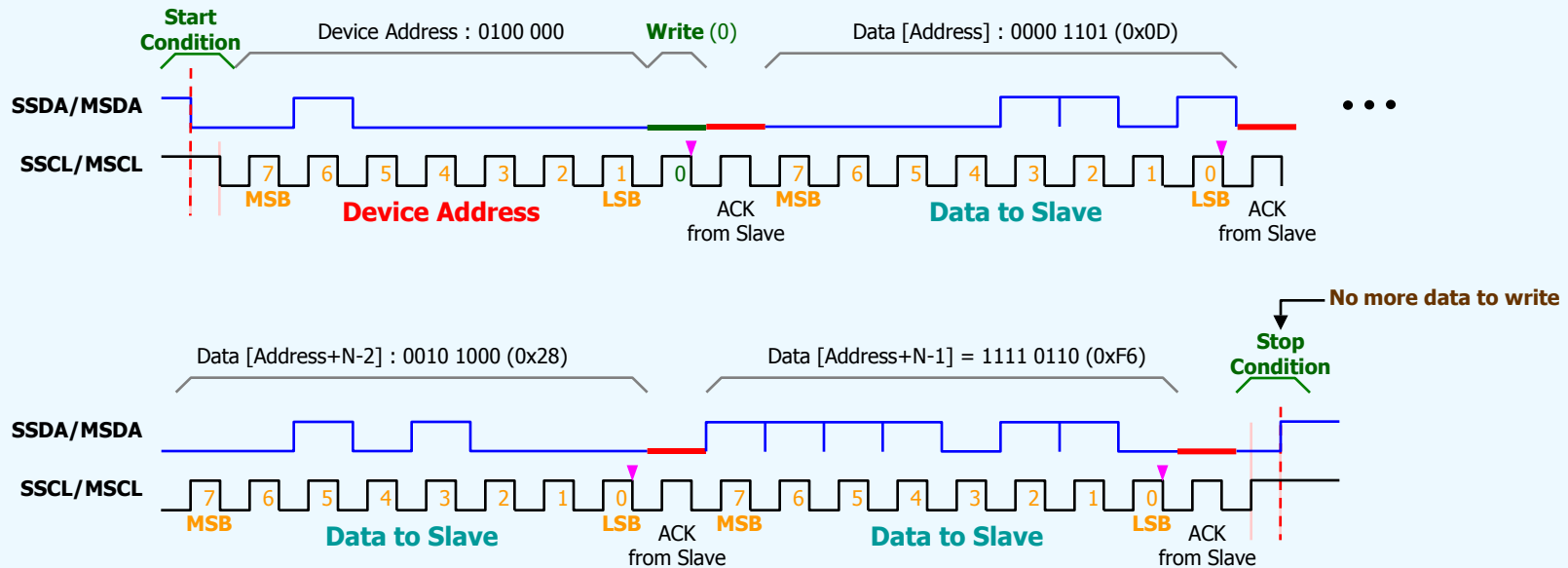


▼ : I<sup>2</sup>C Master/Slave Interrupt

## 6.12. I<sup>2</sup>C : Slave & Master Timing (7/7)

### ◆ Multi (N) Bytes Write Timing without Memory Address

- ✓ I2C\_SCON.1 (MODE) / I2C\_MCON.1 (MODE) = 1 (Mode 1, No Memory Address).



# 6.13. Interrupt : 13 Sources / 2-level Priority

- ◆ 13 Interrupt Sources
  - ✓ Timer 0/1, UART, ADC, WDT, LVD, 2-I<sup>2</sup>C, PWM, 4 External
- ◆ 2-level Interrupt Priority

**[Interrupt Vector Address]**

Interrupt Sources	Address	Priority Level
LVD	0033h	Highest
$\overline{\text{INT0}}$	0003h	2 Levels
TF0	000Bh	2 Levels
$\overline{\text{INT1}}$	0013h	2 Levels
TF1	001Bh	2 Levels
RI+TI	0023h	2 Levels
ADC	003Bh	2 Levels
INT2	0043h	2 Levels
$\overline{\text{INT3}}$	004Bh	2 Levels
I <sup>2</sup> C Master	0053h	2 Levels
I <sup>2</sup> C Slave	005Bh	2 Levels
WDT	0063h	2 Levels
PWM	006Bh	2 Levels

**↑ HIGH PRIORITY** (indicated by a red arrow on the left)

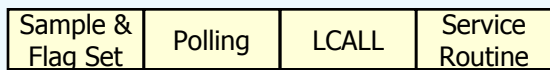
**↓ LOW** (indicated by an orange arrow on the left)

**NMI** (Non-Maskable Interrupt) is associated with the LVD source.

\* Interrupt related to SFR (refer to Appendix B : SFR Description)

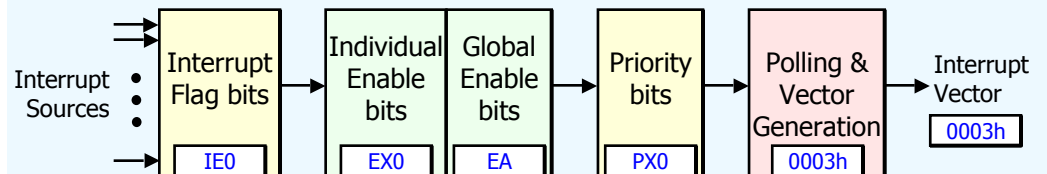
✓ <b>TCON</b> (88h)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
✓ <b>EXIF</b> (91h)	-	-	IE3	IE2	XT/RG	RGMD	RGSL	BGS
✓ <b>SCON</b> (98h)	-	-	-	REN	-	-	TI	RI
✓ <b>IE</b> (A8h)	EA	EADC	-	ES	ET1	EX1	ET0	EX0
✓ <b>IP</b> (B8h)	-	PADC	-	PS	PT1	PX1	PT0	PX0
✓ <b>EIE</b> (E8h)	-	-	EPWM	EWDT	EI2C_S	EI2C_M	EX3	EX2
✓ <b>EIP</b> (F8h)	-	-	PPWM	PWDT	PI2C_S	PI2C_M	PX3	PX2
✓ <b>WDCON</b> (D8h)	WD1	WD0	EPFI	PFI	WDIF	WTRF	EWT	RWT
✓ <b>PWMCON</b> (DCh)	POSEL	PS2_P0	PS1_P0	PS0_P0	-	PWMF	CLR_P0	RUN_P0
✓ <b>I2C_SCON</b> (C0h)	-	WR	RD	BUSY	-	I2C_SIF	MODE	RUN
✓ <b>I2C_MCON</b> (C8h)	-	-	-	I2C_MIF	OP	BYPASS	MODE	RUN
✓ <b>ADCON</b> (EFh)	AD_EN	AD_REQ	AD_END	ADCF	-	ADIV	SAR1	SAR0

**[Response Sequence]**

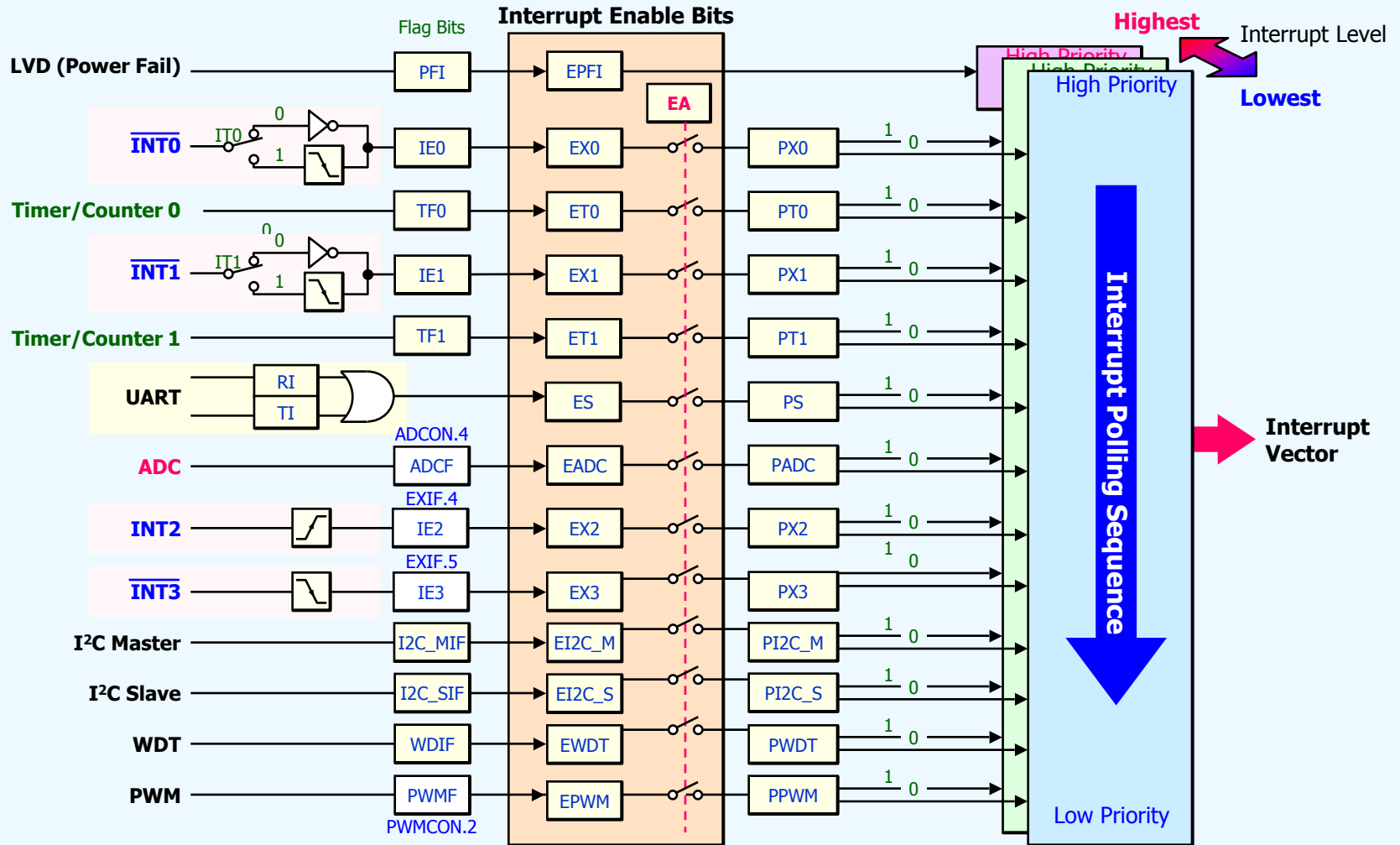


↑ Last Cycle & High Priority & Not-update Interrupt Register

**[Interrupt Vector Generation Flow]**



# 6.13. Interrupt Functional Description



## 6.14. Reset Circuit : Three Reset Sources

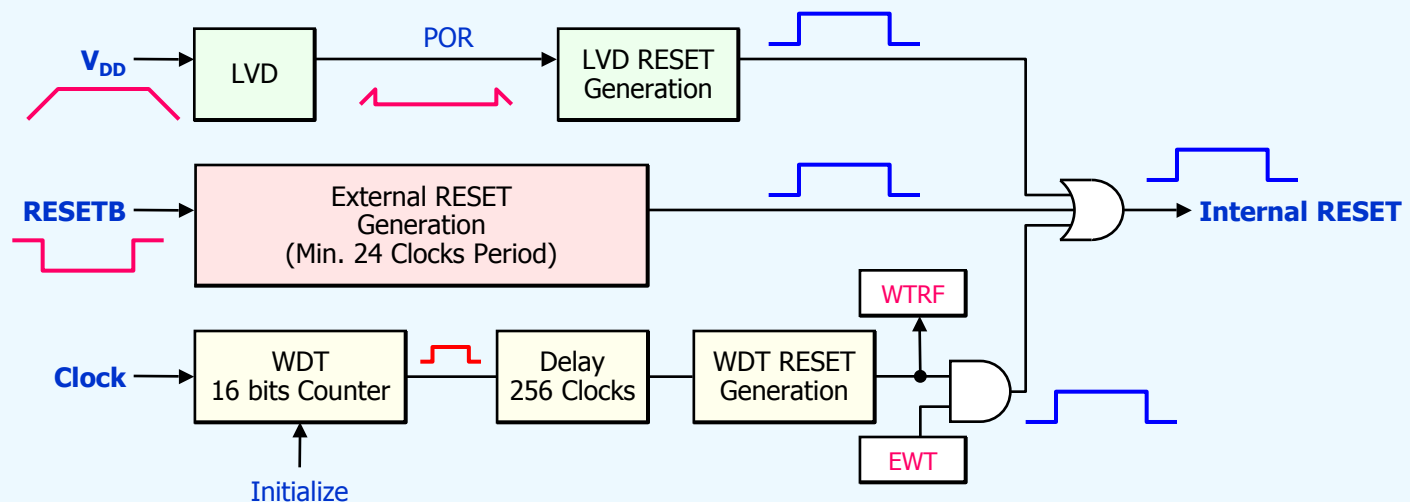
- ◆ LVD(POR) Reset
  - ✓ Power-on Reset when Power-Up.
  - ✓ Power-fail Reset under  $V_{RST}$
- ◆ External RESET Pin
  - ✓ RESETB Pin must hold "L" for min. 24 clocks period.
  - ✓ Ring OSC. must be running.
- ◆ WDT Reset : Enabled or disabled by S/W

✓ **WDCON** (D8h) : Watchdog Timer Control Register

WD1	WD0	EPFI	PFI	WDIF	WTRF	EWT	RWT
R/W(1)	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

R/W(1) R/W(1) R/W(0) R/W(1) R/W(0) R/W(0) R/W(0) R/W(0)

- WTRF : Watchdog Timer Reset Flag. Only cleared by S/W.
- EWT : Watchdog Timer Reset Enable.



# 6.15. Clock Circuit

- ◆ 2 System Clock Sources : Ring OSC. or External Crystal
- ◆ Default System Clock is Ring OSC.
- ◆ Fast Wake-up from Power-down Mode using Ring OSC.

Control Flag				System Clock	Status Bit	
XT/RG	XTOFF	RINGON	RGSL		RGMD	XTUP
1	0	X	X	Crystal OSC.	0	1
0	X	1	X	Ring OSC.	1	0/1
1	0	X	0	Crystal OSC. (during Power-down Wake-up)	0	0
0	X	1	1	Ring OSC. (during Power-down Wake-up)	1	0

✓ **EXIF** (91h) : External Interrupt Flag Register

-	-	IE3	IE2	XT/RG	RGMD	RGSL	BGS
R/W(0)	R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(0)	R/W(1)	R/W(1)

✓ **OSCICN** (BEh) : Internal Ring Oscillator Control Register

-	-	-	-	DIV2	RINGON	DIV1	DIV0
R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(0)	R/W(0)

✓ **STATUS** (C5h) : Crystal Status Register

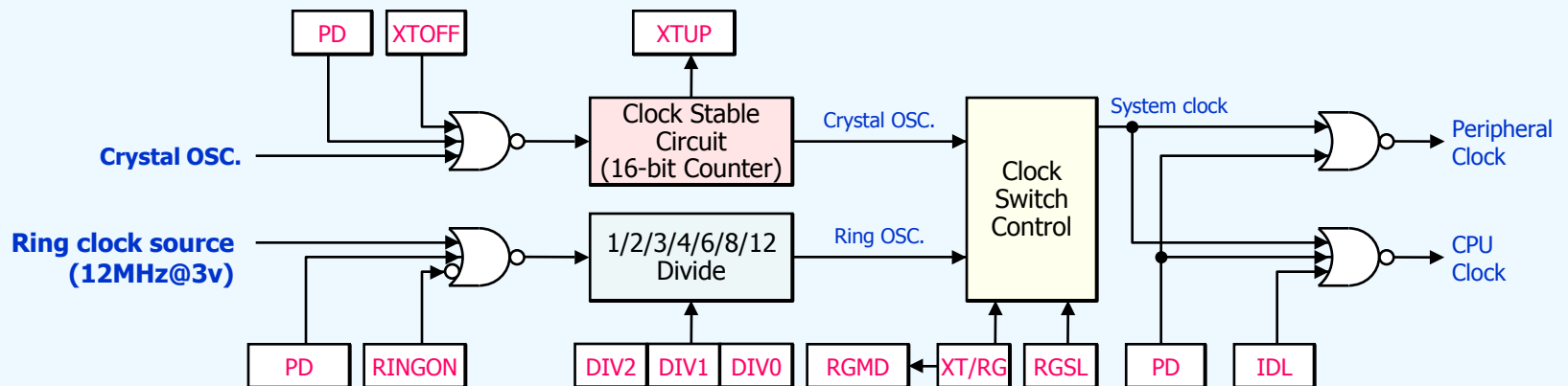
-	-	-	XTUP	-	-	-	-
R(0)	R(0)	R(0)	R(0)	R(0)	R(0)	R(0)	R(0)

✓ **PMR** (C4h) : Power Management Control Register

-	-	-	-	XTOFF	-	-	-
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ **PCON** (87h) : Power Control Register

SMOD1	-	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)





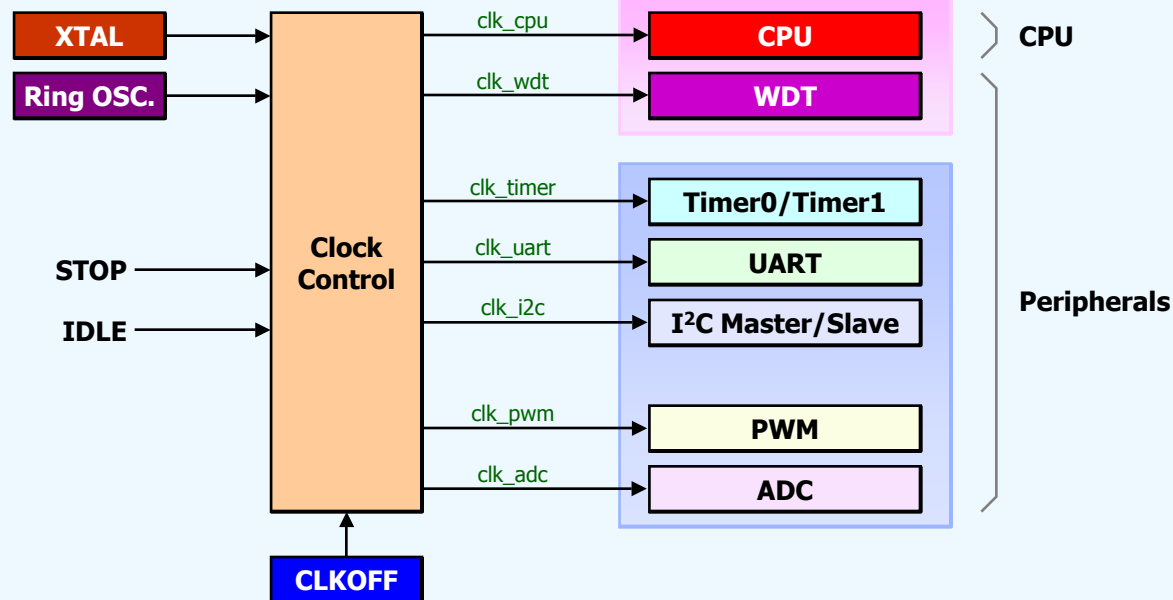
## 6.16. Power Management : Clock Circuit

- ◆ When MCU is in IDLE mode, CPU will stop and all the peripherals will run as below.
  - ✓ WDT, Timer, UART, I<sup>2</sup>C, PWM, & ADC
- ◆ When MCU is in STOP mode, CPU & all the peripherals will stop.
- ◆ The below peripherals will be stopped with CLKOFF SFR.
  - ✓ Timer0/1, UART, I<sup>2</sup>C, PWM, & ADC
  - ✓ Refer to CLKOFF SFR.

✓ **CLKOFF** (94h) : Peripheral Clock Control Register

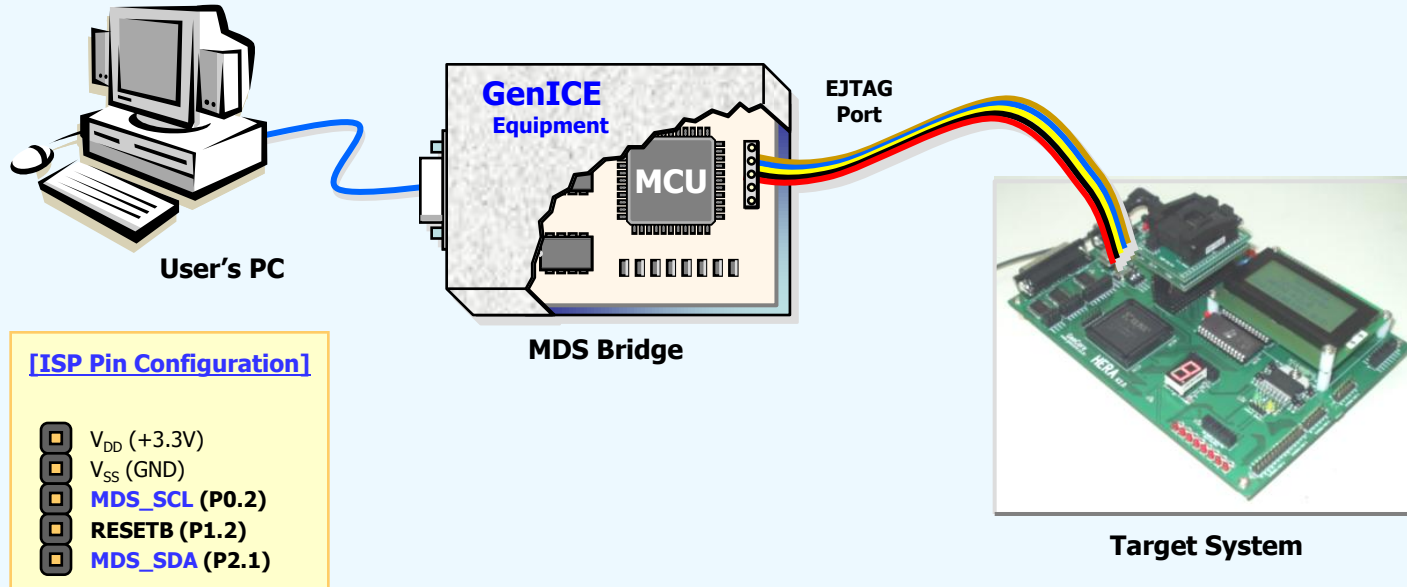
-	-	OFF_T01	OFF_UART	-	OFF_I2C	OFF_PWM	OFF_ADC
		R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)

- OFF\_ADC : ADC Block OFF. 1 = ADC block will stop.
- OFF\_PWM : PWM Block OFF. 1 = PWM block will stop.
- OFF\_I2C : I<sup>2</sup>C Block OFF. 1 = I<sup>2</sup>C master/slave block will stop.
- OFF\_UART : UART Block OFF. 1 = UART block will stop.
- OFF\_T01 : Timer0/1 Block OFF. 1 = Timer0 and Timer1 will stop.



## 6.17. ISP & Debugging

- ◆ Code memory (7KBytes) can be programmed using EJTAG in target system.
  - ✓ FLASH : 0x0000 ~ 0x1BFF (7,168 Bytes)
- ◆ EEPROM (1KBytes) can be programmed using EJTAG in target system.
  - ✓ EEPROM : 0x1C00 ~ 0x1FFF (1,024 Bytes)
- ◆ Debugging using GENICE



- ◆ If the operating voltage of target board is +5V, don't connect V<sub>DD</sub> cable pin of GenICE52 equipment.
- ◆ Please, individually supply the voltage (+5V) to target board.
- ◆ The other cable pins of GenICE52 are +5V compatible.

## 6.17. ISP : Command Set

Command	Function
Blank	<ul style="list-style-type: none"> <li>◆ Check the blank status of the device currently connected.</li> </ul>
Erase Chip	<ul style="list-style-type: none"> <li>◆ Performs an erase chip, the device's memory, both code and data.                             <ul style="list-style-type: none"> <li>• Code : FLASH</li> <li>• User data : EEPROM</li> <li>• Information data : Lock bits, RING option, PGM/ERS time (ISP)</li> </ul> </li> </ul>
	<ul style="list-style-type: none"> <li>◆ The device will be blank and in a programmable state.</li> </ul>
Read Code/EEPROM	<ul style="list-style-type: none"> <li>◆ Reads in the device's memory.</li> </ul>
	<ul style="list-style-type: none"> <li>◆ The results from the read are loaded into the CORERIVER ISP software's buffer and displayed on the screen.</li> </ul>
Write Chip/EEPROM	<ul style="list-style-type: none"> <li>◆ Writes all memory locations in the CORERIVER ISP software's buffer out to the device's memory.</li> </ul>
Verify Chip	<ul style="list-style-type: none"> <li>◆ Compares the CORERIVER ISP software buffer with the device's internal memory.</li> </ul>
	<ul style="list-style-type: none"> <li>◆ If the buffers are found to be exact replicas of the device's memory, a success result is returned.</li> </ul>
	<ul style="list-style-type: none"> <li>◆ If there are any differences, a failure result is returned along with the total number of mismatched bytes.</li> </ul>

## 6.17. IAP ( In Application Programming)

- ◆ Code memory(7KB) & EEPROM(1KB) can be programmed during the operation of MCU.
- ◆ Program time : approximately 5.0 ms
- ◆ Program unit : 1 Byte
- ◆ IAP SFR

✓ **EEAEN** (FFh) : IAP Routine Access Enable Register

-	-	-	-	-	-	-	EAEN
---	---	---	---	---	---	---	------

R/W(0)

- EAEN : IAP Routine Access Enable

✓ **DPL** (82h) : Data Pointer Low Register

DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

✓ **DPH** (83h) : Data Pointer High Register

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

✓ **ACC/A** (E0h) : Accumulator

ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

✓ **B** (F0h) : B Register

B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
-----	-----	-----	-----	-----	-----	-----	-----

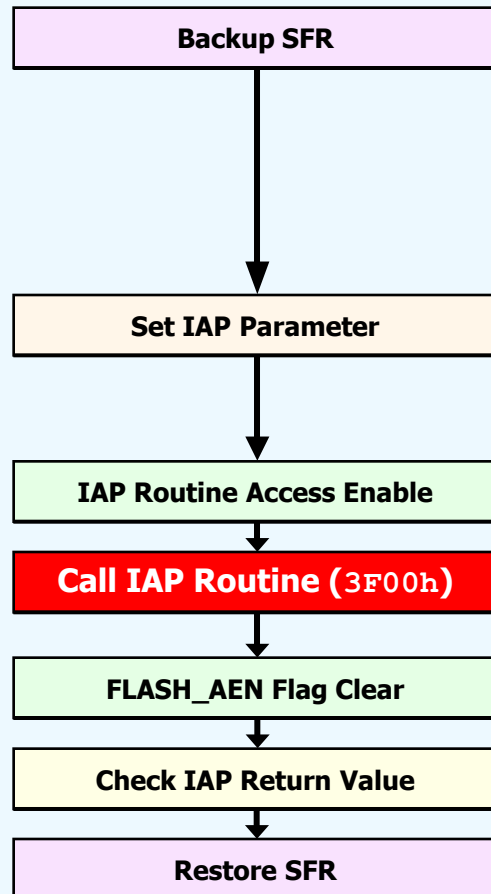
R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## 6.17. IAP : Function Set

- ◆ IAP call address
  - ✓ 3F00h
- ◆ IAP return values
  - ✓ Success :[ACC] 83h or 86h
  - ✓ Program Fail :[ACC] FCh
  - ✓ Address Fail :[ACC] FDh
  - ✓ Lock Fail :[ACC] FEh
  - ✓ Command Fail :[ACC] FFh
- ◆ Before calling IAP function, any interrupt must be disabled.
- ◆ Before calling IAP function, EAEN flag in EEAEN SFR must be set.
  - ✓ **Only use ORL/ANL assembly instruction to set or reset EAEN flag.**
- ◆ After executing IAP function, the value of PSW SFR can be changed.
- ◆ Any interrupt service routine will not be executed timely since the CPU is suspended for tens of milliseconds during executing an IAP function (Program/Erase).

Call Address	Command	Function	B	ACC	DPTR	Return Value (ACC)
3F00h	Program	Program Code Byte	3h	Code to be programmed	FLASH address	83h/FCh/FDh/FEh/FFh
		Program EEPROM Byte	6h	Data to be programmed	EEPROM Address	86h/FCh/FDh/FEh/FFh

## 6.17. IAP : Coding Flow



### [ Example Code : IAP Program for FLASH ]

```
PUSH A           ; backup acc
PUSH B           ; backup b
PUSH DPL         ; backup dptr
PUSH DPH
PUSH R6          ; backup R6
MOV R1, IE      ; backup IE SFR
CLR IE.7        ; Interrupt disable
```

```
MOV B, #03h     ; IAP Function setting
MOV A, #55h     ; Programmed Data
MOV DPTR, #01000h ; Programmed Address
```

```
ORL EEAEN, #01h ; IAP routine access enable
```

```
CALL 3F00h     ; Call IAP routine
```

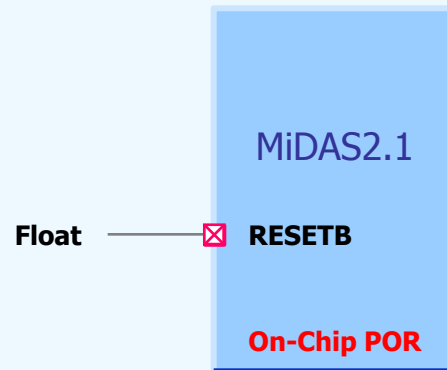
```
ANL EEAEN, #0FEh ; IAP routine access disable
```

```
CJNE A, #83h, IAP_FAIL ; Check return message
```

```
MOV IE, r1     ; restore IE SFR
POP R6         ; restore acc, b, dptr, R6
POP DPH
POP DPL
POP B
POP A
```

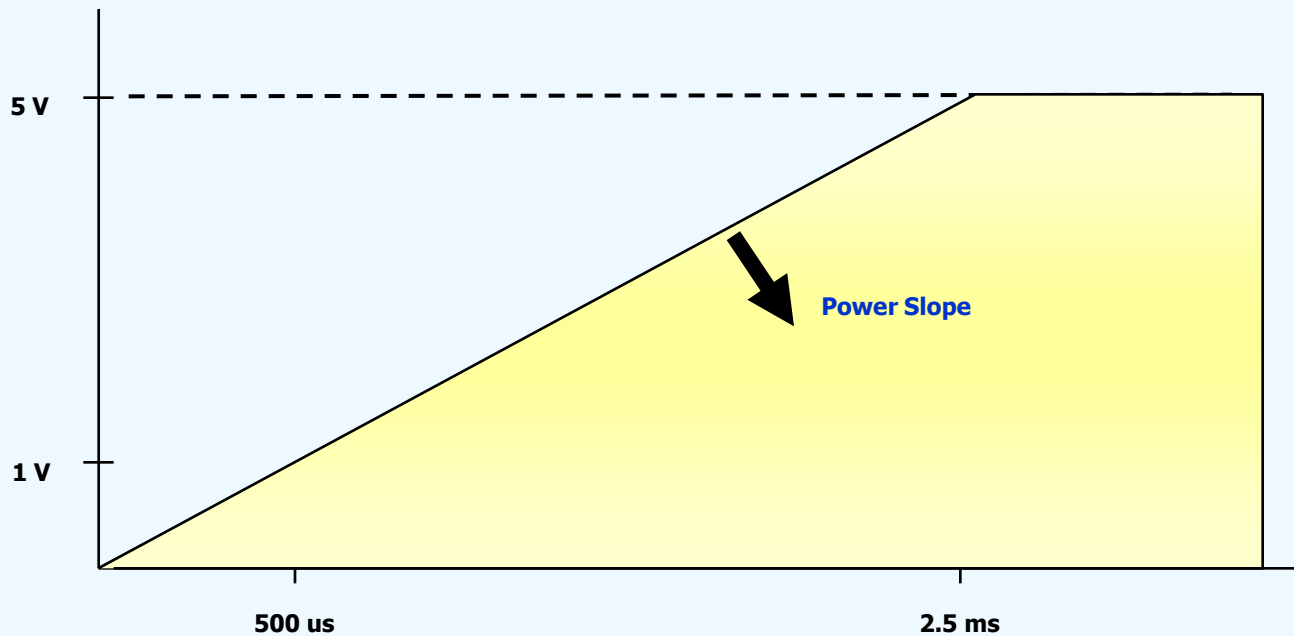
## 7. Strong Point : On-Chip POR

- ◆ On-Chip POR (Power On Reset) can reduce the system cost by removing needless capacitor or even resistor.
- ◆ Even of RESETB pin is float state, if is no problem.



## 8. Recommended Power Slope

- ◆ The supply voltage slope must be in the range from 0.0V/us to 1.0V/500us. (5V/2.5ms)  
(That is, the supply voltage should be increasing monotonically until it reaches to the normal range.)



## 9. Absolute Maximum Ratings

Items	Conditions	Ranges
Voltage on any pin relative to Ground	-	-0.5V to ( $V_{DD}+0.5V$ )
Voltage in $V_{DD}$ relative to Ground	-	-0.5V to 6.5V
Output Voltage	-	-0.5V to ( $V_{DD}+0.5V$ )
Output Current High	One I/O pin active	-25mA
	All I/O pin active	-100mA
Output Current Low	One I/O pin active	+30mA
	All I/O pin active	+150mA
Operating Temperature	-	-40 °C to 120 °C
Storage Temperature	-	-65 °C to +150 °C
Soldering Temperature	-	260 °C for 10 seconds

# 10. DC Characteristics

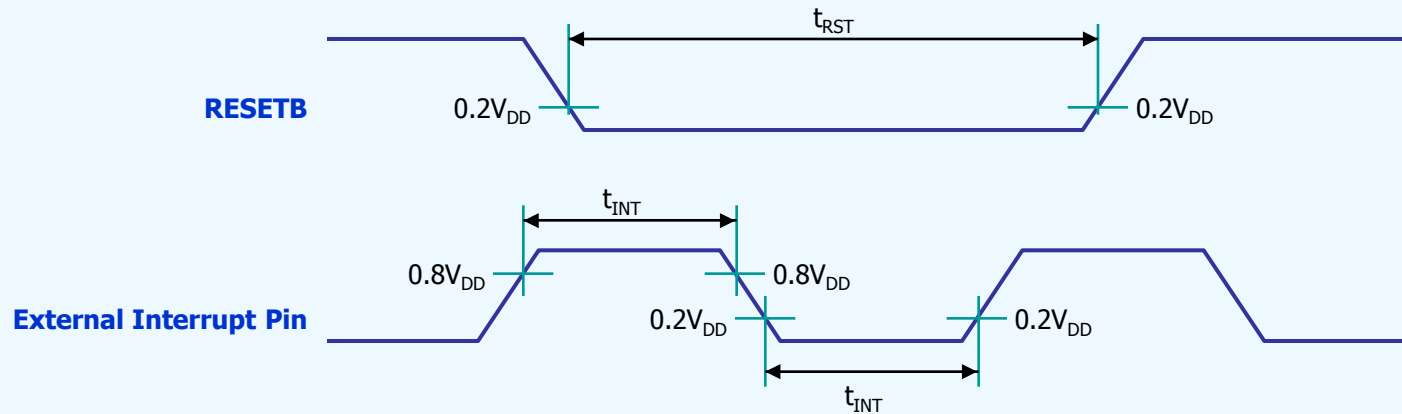
\* TA = -40 °C ~ +125 °C, V<sub>DD</sub> = 2.2V ~ 5.5V unless otherwise specified.

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input Low Voltage	V <sub>IL1</sub>	RESETB,P0, P1,P2,P3	V <sub>DD</sub> = 2.2V~5.5V	-0.5	-	0.2V <sub>DD</sub> -0.1	V
	V <sub>IL2</sub>	XTAL1, XTAL2		-0.5	-	0.3V <sub>DD</sub>	
Input high Voltage	V <sub>IH1</sub>	P0, P1,P2,P3,RESETB	V <sub>DD</sub> = 2.2V~5.5V	0.2V <sub>DD</sub> +1.0	-	V <sub>DD</sub> +0.5	V
	V <sub>IH2</sub>	XTAL1, XTAL2		0.7V <sub>DD</sub>	-	V <sub>DD</sub> +0.5	
Output Low Voltage	V <sub>OL</sub>	ALL pin	I <sub>OL</sub> = 20mA @V <sub>DD</sub> =5V	-	-	0.3V <sub>DD</sub>	V
Output High Voltage	V <sub>OH</sub>	ALL pin	I <sub>OH</sub> = -15mA @V <sub>DD</sub> =5V (I <sub>OH</sub> = -2.5mA @V <sub>DD</sub> =2.6V)	0.7V <sub>DD</sub>	-	-	V
	V <sub>OHP</sub>	Pull-up	I <sub>OH</sub> = -140uA @V <sub>DD</sub> =5V (I <sub>OH</sub> = -20uA @V <sub>DD</sub> =2.6V)	0.7V <sub>DD</sub>	-	-	V
Input Leakage Current	I <sub>IL</sub>	All pins except XTAL1,XTAL2	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	-	±1	μA
Pin Capacitance	C <sub>I0</sub>	All	V <sub>DD</sub> = 5V	-	10	-	pF

# 11. AC Characteristics

\*  $T_A = -20\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$  unless otherwise specified.

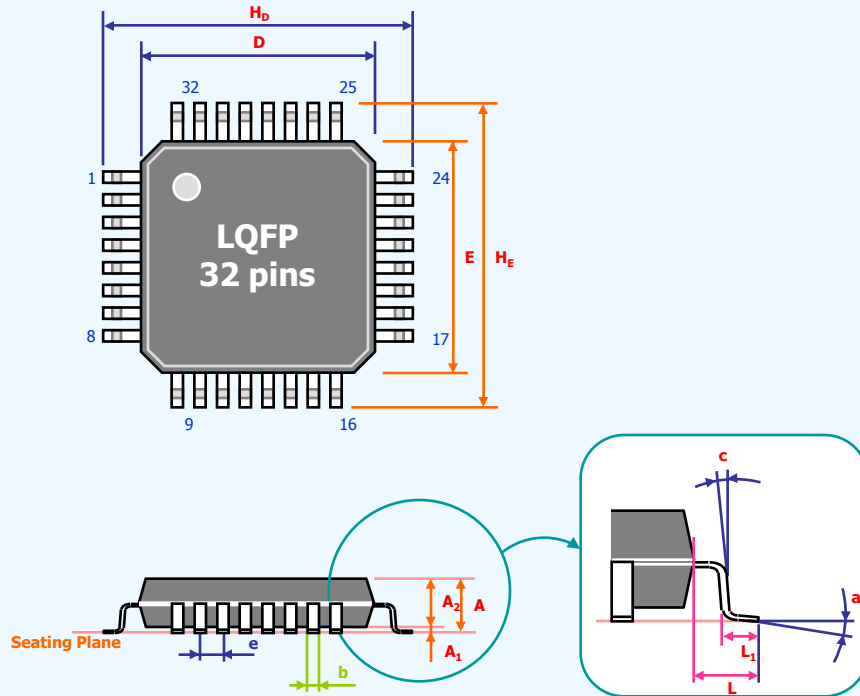
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Operating Frequency	$F_{OSC}$	XTAL1, XTAL2	$V_{DD} = 5V \pm 10\%$	1	-	20	MHz
			$V_{DD} = 3V \pm 10\%$	1	-	12	
RESETB Input Width	$t_{RST}$	RESETB	$V_{DD} = 5V \pm 10\%$	24	-	-	$F_{OSC}$
			$V_{DD} = 3V \pm 10\%$	24	-	-	
External Interrupt Input Width	$t_{INT}$	External Interrupt	$V_{DD} = 5V \pm 10\%$	4	-	-	$F_{OSC}$
			$V_{DD} = 3V \pm 10\%$	4	-	-	



# 12. ADC Specifications

Parameter	Symbol	Conditions	Value			Unit	
			Min.	Typ.	Max.		
Supply Voltage	$V_{DDADC}$	-	2.2	-	5.5	V	
Input Voltage	$V_{INADC}$	-	$V_{SS}$	-	$V_{DD}$	V	
Resolution	$RES_{ADC}$	-	-	10	-	bit	
Operating Frequency	$F_{ADC}$	$V_{DD} = 4.5V \sim 5.5V$ $V_{DD} = 2.2V \sim 3.3V$	-	-	10 5	MHz	
Conversion Time	$t_{ADC}$	-	-	$96 / F_{ADC}$	-	s	
Overall Accuracy	$OA_{ADC}$	$V_{DD} = 5V, F_{ADC} = 10MHz$ $V_{DD} = 3V, F_{ADC} = 5MHz$	-	$\pm 2$	$\pm 4$	LSB	
Integral Nonlinearity	$INL_{ADC}$	$V_{DD} = 5V, F_{ADC} = 10MHz$ $V_{DD} = 3V, F_{ADC} = 5MHz$	-	$\pm 2$	$\pm 4$	LSB	
Differential Nonlinearity	$DNL_{ADC}$	$V_{DD} = 5V, F_{ADC} = 10MHz$ $V_{DD} = 3V, F_{ADC} = 5MHz$	-	$\pm 0.5$	$\pm 1$	LSB	
Zero Input Error	$ZIE_{ADC}$	$V_{DD} = 5V, F_{ADC} = 10MHz$ $V_{DD} = 3V, F_{ADC} = 5MHz$	-	$\pm 2$	$\pm 4$	LSB	
Full Scale Error	$FSE_{ADC}$	$V_{DD} = 5V, F_{ADC} = 10MHz$ $V_{DD} = 3V, F_{ADC} = 5MHz$	-	$\pm 2$	$\pm 4$	LSB	
Analog Input Capacitance	$C_{INADC}$	-	-	10	15	pF	
ADC Current	Active	$I_{ADC}$	$V_{DD} = 5V, F_{ADC} = 10MHz$	-	1	2	mA
			$V_{DD} = 3V, F_{ADC} = 5MHz$	-	0.3	0.6	
	Power-down		$V_{DD} = 5V$	-	-	100	nA

# 13. Package Dimensions : 32-LQFP

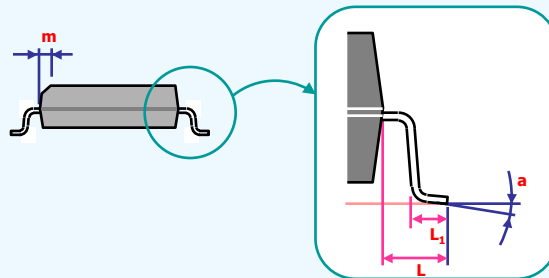
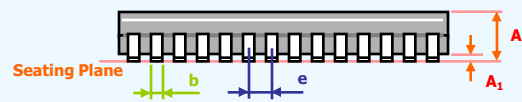
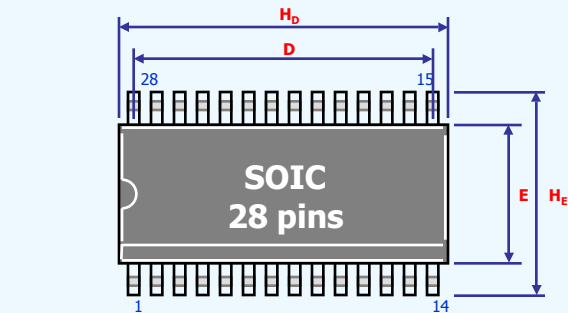


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A <sub>1</sub>	0.002	-	0.006	0.05	-	0.15
A <sub>2</sub>	0.053	-	0.057	1.35	-	1.45
b	0.012	0.015	0.018	0.30	0.38	0.45
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.0315 BSC			0.80 BSC		
H <sub>D</sub>	0.344	0.354	0.364	8.75	9.00	9.25
H <sub>E</sub>	0.344	0.354	0.364	8.75	9.00	9.25
L	-	0.039	-	-	1.00	-
L <sub>1</sub>	0.018	-	0.029	0.45	-	0.75
a	0°	-	7°	0°	-	7°
c	0°	-	-	0°	-	-

### Notes:

1. Dimension D \* E do not include interlead flash.
2. Dimension b, dose not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

# 13. Package Dimensions : 28-SOIC

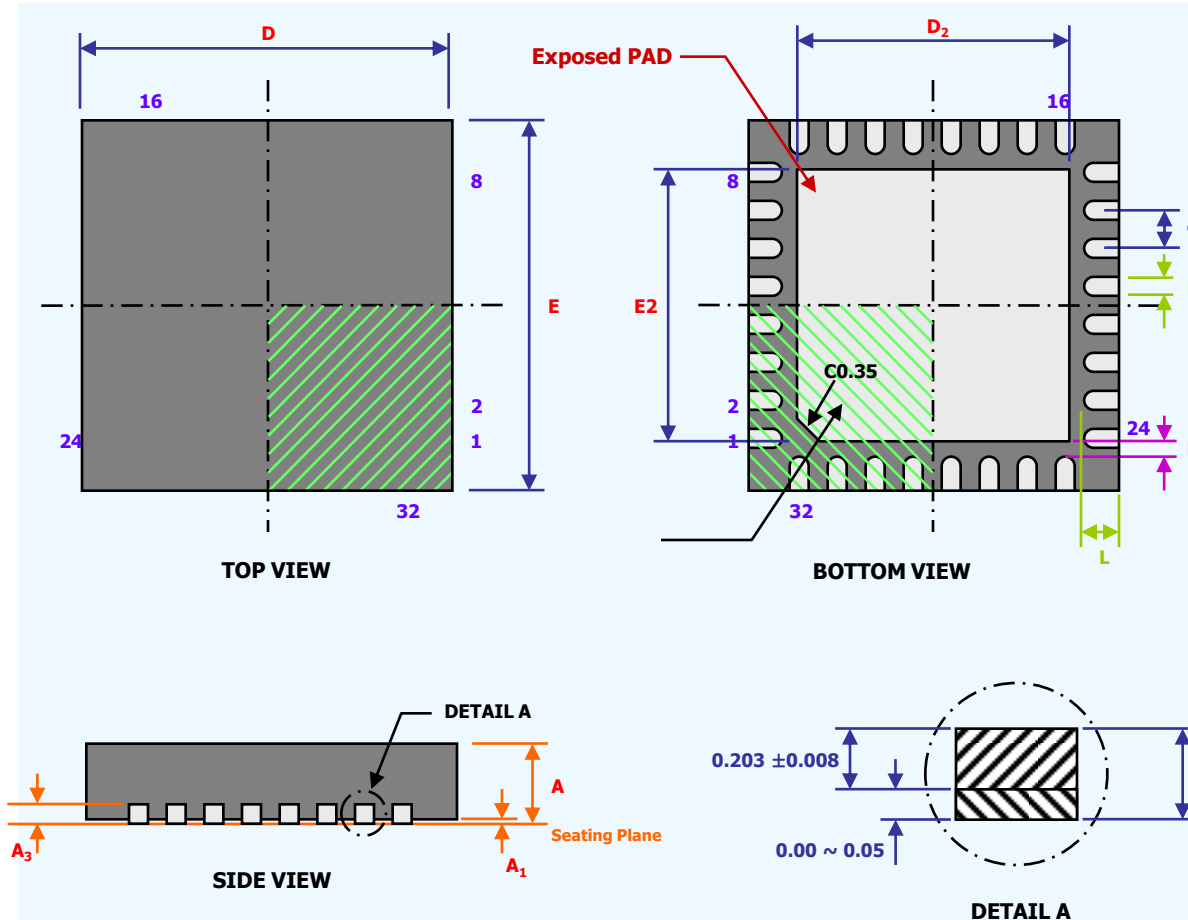


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.093	0.099	0.104	2.35	2.45	2.65
A <sub>1</sub>	0.004	0.008	0.012	0.10	0.20	0.30
b	0.014	0.016	0.019	0.35	0.42	0.49
D	-	0.65	-	-	16.51	-
E	0.291	0.295	0.299	7.40	7.50	7.60
H <sub>b</sub>	0.697	0.705	0.713	17.70	17.90	18.10
H <sub>E</sub>	0.404	0.411	0.419	10.26	10.45	10.65
L	0.057	0.058	0.060	1.43	1.48	1.53
L <sub>1</sub>	0.034	0.038	0.042	0.86	0.96	1.07
a	0°	-	8°	0°	-	8°
e	0.050 BSC			1.27 BSC		
m	0.020	0.025	0.030	0.50	0.62	0.75

**Notes:**

1. Dimension D Max. & S include mold flash or tie bar Burns.
2. Dimension E<sub>1</sub> dose not include interlead flash.
3. Dimension D & E<sub>1</sub> include mold mismatch and are determined at the mold parting line.
4. Dimension B<sub>1</sub> does not include dambar protrusion/intrusion.
5. General appearance spec. should be based on final visual inspection spec.

# 13. Package Dimensions : 32-QFN



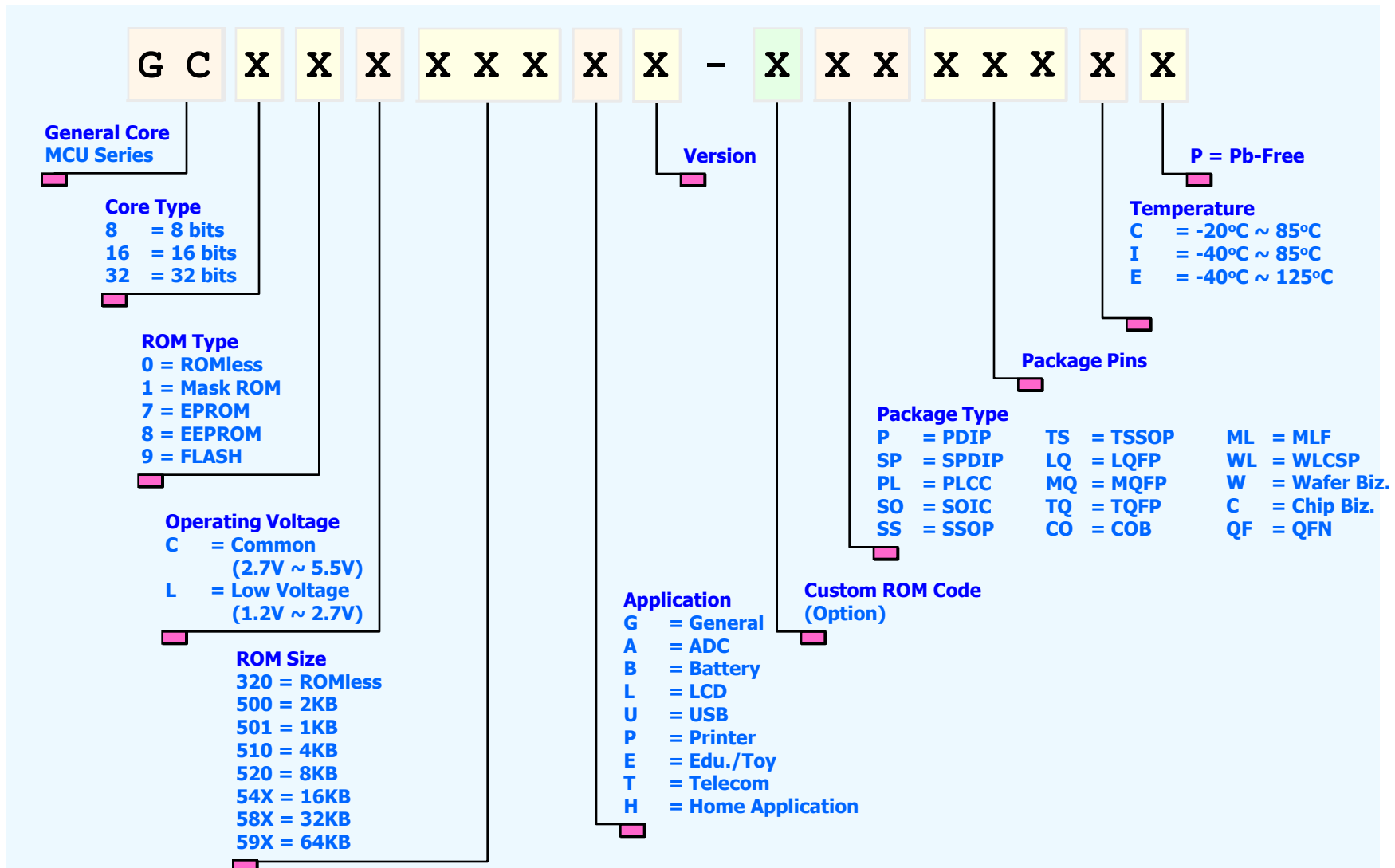
[32-QFN]

Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A <sub>1</sub>	0.00	0.02	0.05
A <sub>3</sub>	0.20 REF		
D	5.00 BSC		
E	5.00 BSC		
D <sub>2</sub>	3.35	3.45	3.55
E <sub>2</sub>	3.35	3.45	3.55
b	0.20	0.25	0.30
e	0.50 REF		
L	0.30	0.40	0.50
K	0.20	-	-

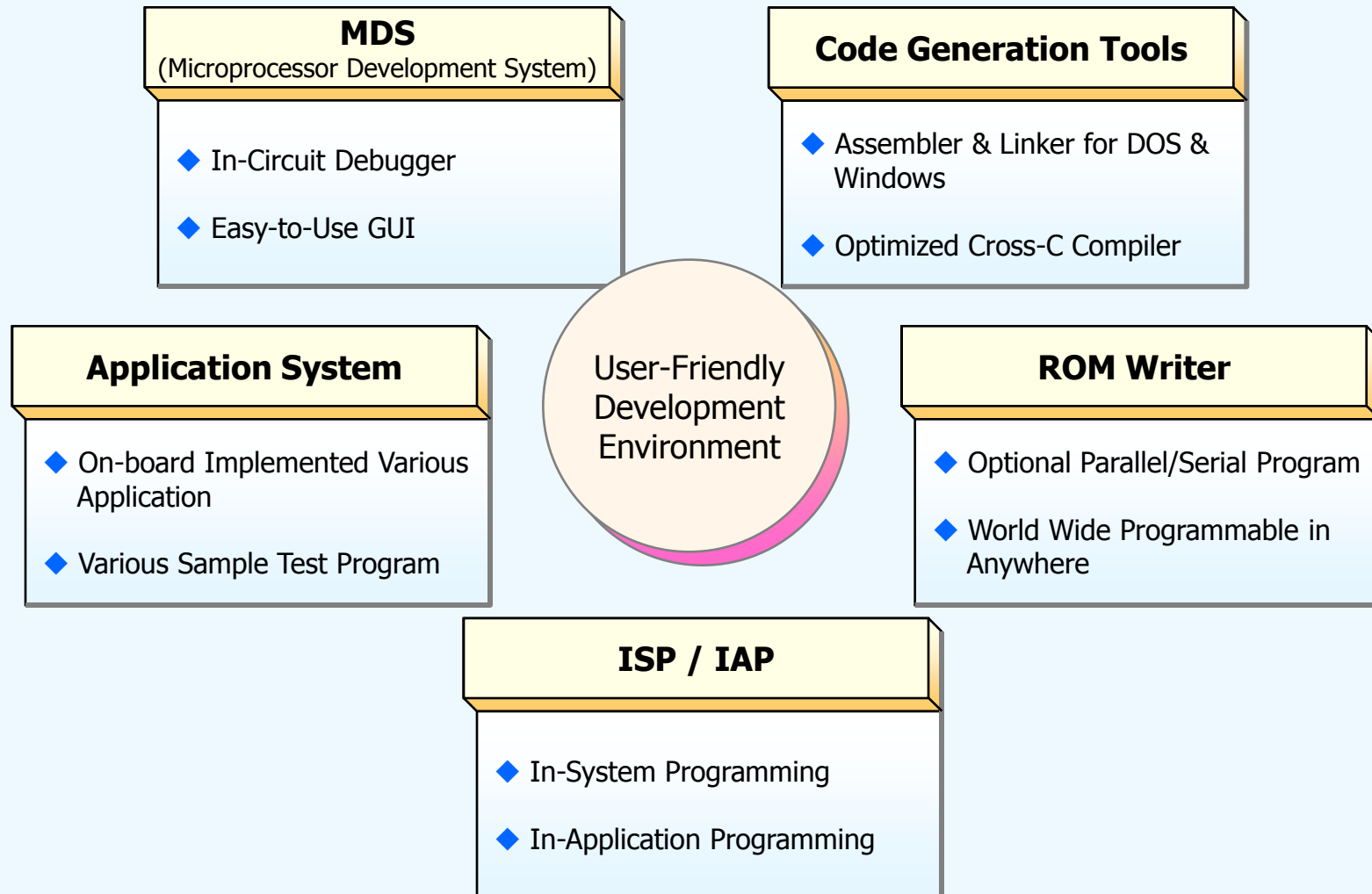
**Notes:**

1. All Dimension are in mm. Angles in Degrees.
  2. Pin 1 visual index feature may vary, but must be located within the hatched area.
  4. Package is saw singulated.
  5. Refer JEDEC MO-220.
  6. BSC : Basic Dimension. Theoretically exact value shown without tolerances.
- REF : Reference Dimension, Usually without tolerance, for information purpose only.

# 14. Product Numbering System



# 15. Supporting tools



# Appendix A : Instruction Set (1/19)

◆ Note on Instruction Set and Addressing Modes

Notation	Descriptions
<b>Rn</b>	Register R0 ~ R7 of the currently selected Register Bank (RB0 ~ RB3).
<b>direct</b>	The address of 8-bit internal data location. This could be an IRAM location (0x00 ~ 0x7F; 128 bytes) or a SFR (0x80 ~ 0xFF).
<b>@Ri</b>	8-bit IRAM location (0x00 ~ 0xFF; 256 bytes) addressed indirectly through register <b>R0</b> or <b>R1</b> .
<b>#data</b>	8-bit constant included in instruction.
<b>#data16</b>	16-bit constant included in instruction.
<b>addr16</b>	16-bit destination address. Used by <b>LCALL</b> & <b>LJMP</b> . The branch can be anywhere within the 64kbytes program memory address space. (MiDAS2.1 Family : 7kbytes program memory)
<b>addr11</b>	11-bit destination address. Used by <b>ACALL</b> & <b>AJMP</b> . The branch will be within the same 2kbytes page of program memory as the first byte of the following instruction.
<b>rel</b>	Signed (2's complement number) 8-bit offset byte. Used by <b>SJMP</b> and all conditional jumps. Range is -128 to +127 byte relative to first byte of the following instruction.
<b>Bit</b>	Direct addressed bit n IRAM of SFR.

# Appendix A : Instruction Set (2/19)

**ADD A, <src-byte>**

## Add

**ADD A, Rn**

**Operation :** (A) ← (A) + (Rn)

**ADD A, @Ri**

**Operation :** (A) ← (A) + ((Ri))

**ADD A, direct**

**Operation :** (A) ← (A) + (direct)

**ADD A, #date**

**Operation :** (A) ← (A) + data

1 cycle = 4 clocks

**Encoding :** HEX: 28h, #bytes: 1, Cycles: 1

0 0 1 0 1 r r r

**Encoding :** HEX: 26h, #bytes: 1, Cycles: 1

0 0 1 0 0 1 1 i

**Encoding :** HEX: 25h, #bytes: 2, Cycles: 2

0 0 1 0 0 1 0 1

direct addr

**Encoding :** HEX: 24h, #bytes: 2, Cycles: 2

0 0 1 0 0 1 0 0

immediate data

**ADDC A, <src-byte>**

## Add with Carry

**ADDC A, Rn**

**Operation :** (A) ← (A) + (C) + (Rn)

**ADDC A, @Ri**

**Operation :** (A) ← (A) + (C) + ((Ri))

**ADDC A, direct**

**Operation :** (A) ← (A) + (C) + (direct)

**ADDC A, #date**

**Operation :** (A) ← (A) + (C) + data

**Encoding :** HEX: 38h, #bytes: 1, Cycles: 1

0 0 1 1 1 r r r

**Encoding :** HEX: 36h, #bytes: 1, Cycles: 1

0 0 1 1 0 1 1 i

**Encoding :** HEX: 35h, #bytes: 2, Cycles: 2

0 0 1 1 0 1 0 1

direct addr

**Encoding :** HEX: 34h, #bytes: 2, Cycles: 2

0 0 1 1 0 1 0 0

immediate data

# Appendix A : Instruction Set (3/19)

**SUBB A, <src-byte>**

## Subtract with Borrow

**SUBB A, Rn**

**Operation :** (A)  $\leftarrow$  (A) - (C) - (Rn)

**SUBB A, @Ri**

**Operation :** (A)  $\leftarrow$  (A) - (C) - ((Ri))

**SUBB A, direct**

**Operation :** (A)  $\leftarrow$  (A) - (C) - (direct)

**SUBB A, #data**

**Operation :** (A)  $\leftarrow$  (A) - (C) - data

**INC <byte>**

## Increment

**INC A**

**Operation :** (A)  $\leftarrow$  (A) + 1

**INC Rn**

**Operation :** (Rn)  $\leftarrow$  (Rn) + 1

**INC @Ri**

**Operation :** ((Ri))  $\leftarrow$  ((Ri)) + 1

**INC direct**

**Operation :** (direct)  $\leftarrow$  (direct) + 1

**INC DPTR**

**Operation :** (DPTR)  $\leftarrow$  (DPTR) + 1

**Encoding :** HEX: 98h, #bytes: 1, Cycles: 1

1	0	0	1	1	r	r	r
---	---	---	---	---	---	---	---

**Encoding :** HEX: 96h, #bytes: 1, Cycles: 1

1	0	0	1	0	1	1	i
---	---	---	---	---	---	---	---

**Encoding :** HEX: 95h, #bytes: 2, Cycles: 2

1	0	0	1	0	1	0	1
---	---	---	---	---	---	---	---

direct addr

**Encoding :** HEX: 94h, #bytes: 2, Cycles: 2

1	0	0	1	0	1	0	0
---	---	---	---	---	---	---	---

immediate data

**Encoding :** HEX: 04h, #bytes: 1, Cycles: 1

0	0	0	0	0	1	0	0
---	---	---	---	---	---	---	---

**Encoding :** HEX: 08h, #bytes: 1, Cycles: 1

0	0	0	0	1	r	r	r
---	---	---	---	---	---	---	---

**Encoding :** HEX: 06h, #bytes: 1, Cycles: 1

0	0	0	0	0	1	1	i
---	---	---	---	---	---	---	---

**Encoding :** HEX: 05h, #bytes: 2, Cycles: 2

0	0	0	0	0	1	0	1
---	---	---	---	---	---	---	---

direct addr

**Encoding :** HEX: A3h, #bytes: 1, Cycles: 1

1	0	1	0	0	0	1	1
---	---	---	---	---	---	---	---

# Appendix A : Instruction Set (4/19)

**DEC** <byte>

## Decrement

**DEC** A

**Operation :** (A)  $\leftarrow$  (A) - 1

**DEC** Rn

**Operation :** (Rn)  $\leftarrow$  (Rn) - 1

**DEC** @Ri

**Operation :** ((Ri))  $\leftarrow$  ((Ri)) - 1

**DEC** direct

**Operation :** (direct)  $\leftarrow$  (direct) - 1

**DEC** DPTR

**Operation :** (DPTR)  $\leftarrow$  (DPTR) - 1

**Encoding :** HEX: 14h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	0	0
---	---	---	---	---	---	---	---

**Encoding :** HEX: 18h, #bytes: 1, Cycles: 1

0	0	0	1	1	r	r	r
---	---	---	---	---	---	---	---

**Encoding :** HEX: 16h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	1	i
---	---	---	---	---	---	---	---

**Encoding :** HEX: 15h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	0	1
---	---	---	---	---	---	---	---

direct addr

**Encoding :** HEX: A5h, #bytes: 1, Cycles: 1

1	0	1	0	0	1	0	1
---	---	---	---	---	---	---	---

**MUL** AB

## Multiply

**Operation :** (A)<sub>7-0</sub>  $\leftarrow$  (A)  $\times$  (B)  
(B)<sub>15-8</sub>

**Encoding :** HEX: A4h, #bytes: 1, Cycles: 3

1	0	1	0	0	1	0	0
---	---	---	---	---	---	---	---

**DIV** AB

## Divide

**Operation :** (A)<sub>15-8</sub>  $\leftarrow$  (A) / (B)  
(B)<sub>7-0</sub>

**Encoding :** HEX: 84h, #bytes: 1, Cycles: 3

1	0	0	0	0	1	0	0
---	---	---	---	---	---	---	---

# Appendix A : Instruction Set (5/19)

DA A

## Decimal-adjust Accumulator for Addition

**Operation :**

```

IF [[ (A3-0) > 9] ∨ [(AC) = 1]]
    THEN (A3-0) ← (A3-0) + 6
IF [[ (A7-4) > 9] ∨ [(C) = 1]]
    THEN (A7-4) ← (A7-4) + 6
    
```

**Encoding :** HEX: D4h, #bytes: 1, Cycles: 1

1	1	0	1	0	1	0	0
---	---	---	---	---	---	---	---

ANL <dest-byte>, <src-byte>

## Logical AND for byte variables

ANL A, Rn

**Operation :** (A) ← (A) ^ (Rn)

ANL A, @Ri

**Operation :** (A) ← (A) ^ ((Ri))

ANL A, direct

**Operation :** (A) ← (A) ^ (direct)

ANL A, #data

**Operation :** (A) ← (A) ^ data

ANL direct, A

**Operation :** (direct) ← (direct) ^ (A)

ANL direct, #data

**Operation :** (direct) ← (direct) ^ data

**Encoding :** HEX: 58h, #bytes: 1, Cycles: 1

0	1	0	1	1	r	r	r
---	---	---	---	---	---	---	---

**Encoding :** HEX: 56h, #bytes: 1, Cycles: 1

0	1	0	1	0	1	1	i
---	---	---	---	---	---	---	---

**Encoding :** HEX: 55h, #bytes: 2, Cycles: 2

0	1	0	1	0	1	0	1	direct addr
---	---	---	---	---	---	---	---	-------------

**Encoding :** HEX: 54h, #bytes: 2, Cycles: 2

0	1	0	1	0	1	0	0	immediate data
---	---	---	---	---	---	---	---	----------------

**Encoding :** HEX: 52h, #bytes: 2, Cycles: 2

0	1	0	1	0	0	1	0	direct addr
---	---	---	---	---	---	---	---	-------------

**Encoding :** HEX: 53h, #bytes: 3, Cycles: 3

0	1	0	1	0	0	1	1	direct addr	immediate data
---	---	---	---	---	---	---	---	-------------	----------------

# Appendix A : Instruction Set (6/19)

**ANL C, <src-bit>**

## Logical AND for bit variables

ANL C, bit

**Operation :** (C)  $\leftarrow$  (C)  $\wedge$  (bit)

ANL C, /bit

**Operation :** (C)  $\leftarrow$  (C)  $\wedge$   $\sim$ (bit)

**Encoding :** HEX: 82h, #bytes: 2, Cycles: 2

1 0 0 0 0 0 1 0

bit addr

**Encoding :** HEX: B0h, #bytes: 2, Cycles: 2

1 0 1 1 0 0 0 0

bit addr

**ORL <dest-byte>, <src-byte>**

## Logical OR for byte variables

ORL A, Rn

**Operation :** (A)  $\leftarrow$  (A)  $\vee$  (Rn)

ORL A, @Ri

**Operation :** (A)  $\leftarrow$  (A)  $\vee$  ((Ri))

ORL A, direct

**Operation :** (A)  $\leftarrow$  (A)  $\vee$  (direct)

ORL A, #data

**Operation :** (A)  $\leftarrow$  (A)  $\vee$  data

ORL direct, A

**Operation :** (direct)  $\leftarrow$  (direct)  $\vee$  (A)

ORL direct, #data

**Operation :** (direct)  $\leftarrow$  (direct)  $\vee$  data

**Encoding :** HEX: 48h, #bytes: 1, Cycles: 1

0 1 0 0 1 r r r

**Encoding :** HEX: 46h, #bytes: 1, Cycles: 1

0 1 0 0 0 1 1 i

**Encoding :** HEX: 45h, #bytes: 2, Cycles: 2

0 1 0 0 0 1 0 1

direct addr

**Encoding :** HEX: 44h, #bytes: 2, Cycles: 2

0 1 0 0 0 1 0 0

immediate data

**Encoding :** HEX: 42h, #bytes: 2, Cycles: 2

0 1 0 0 0 0 1 0

direct addr

**Encoding :** HEX: 43h, #bytes: 3, Cycles: 3

0 1 0 0 0 0 1 1

direct addr

immediate data

# Appendix A : Instruction Set (7/19)

**ORL C, <src-byte>**

## Logical OR for byte variables

ORL C, bit

**Operation :** (C)  $\leftarrow$  (C)  $\vee$  (bit)

ORL C, /bit

**Operation :** (C)  $\leftarrow$  (C)  $\vee$   $\sim$ (bit)

**XRL <dest-byte>, <src-byte>**

## Logical Exclusive-OR for byte variables

XRL A, Rn

**Operation :** (A)  $\leftarrow$  (A)  $\oplus$  (Rn)

XRL A, @Ri

**Operation :** (A)  $\leftarrow$  (A)  $\oplus$  ((Ri))

XRL A, direct

**Operation :** (A)  $\leftarrow$  (A)  $\oplus$  (direct)

XRL A, #data

**Operation :** (A)  $\leftarrow$  (A)  $\oplus$  data

XRL direct, A

**Operation :** (direct)  $\leftarrow$  (direct)  $\oplus$  (A)

XRL direct, #data

**Operation :** (direct)  $\leftarrow$  (direct)  $\oplus$  data

**Encoding :** HEX: 72h, #bytes: 2, Cycles: 2

0 1 1 1 0 0 1 0

bit addr

**Encoding :** HEX: A0h, #bytes: 2, Cycles: 2

1 0 1 0 0 0 0 0

bit addr

**Encoding :** HEX: 68h, #bytes: 1, Cycles: 1

0 1 1 0 1 r r r

**Encoding :** HEX: 66h, #bytes: 1, Cycles: 1

0 1 1 0 0 1 1 i

**Encoding :** HEX: 65h, #bytes: 2, Cycles: 2

0 1 1 0 0 1 0 1

direct addr

**Encoding :** HEX: 64h, #bytes: 2, Cycles: 2

0 1 1 0 0 1 0 0

immediate data

**Encoding :** HEX: 62h, #bytes: 2, Cycles: 2

0 1 1 0 0 0 1 0

direct addr

**Encoding :** HEX: 63h, #bytes: 3, Cycles: 3

0 1 1 0 0 0 1 1

direct addr

immediate Data

# Appendix A : Instruction Set (8/19)

**CLR    A**

**Clear Accumulator**

**Operation :**    (A)     $\leftarrow$  0

**Encoding :**            HEX: E4h, #bytes: 1, Cycles: 1

1	1	1	0	0	1	0	0
---	---	---	---	---	---	---	---

**CLR    <bit>**

**Clear bit**

CLR    C

**Operation :**    (C)     $\leftarrow$  0

**Encoding :**            HEX: C3h, #bytes: 1, Cycles: 1

1	1	0	0	0	0	1	1
---	---	---	---	---	---	---	---

CLR    bit

**Operation :**    (bit)     $\leftarrow$  0

**Encoding :**            HEX: C2h, #bytes: 2, Cycles: 2

1	1	0	0	0	0	1	0
---	---	---	---	---	---	---	---

bit addr
----------

**CPL    A**

**Complement Accumulator**

**Operation :**    (A)     $\leftarrow$   $\sim$ (A)

**Encoding :**            HEX: F4h, #bytes: 1, Cycles: 1

1	1	1	1	0	1	0	0
---	---	---	---	---	---	---	---

**CPL    <bit>**

**Complement bit**

CPL    C

**Operation :**    (C)     $\leftarrow$   $\sim$ (C)

**Encoding :**            HEX: B3h, #bytes: 1, Cycles: 1

1	0	1	1	0	0	1	1
---	---	---	---	---	---	---	---

CPL    bit

**Operation :**    (bit)     $\leftarrow$   $\sim$ (bit)

**Encoding :**            HEX: B2h, #bytes: 2, Cycles: 2

1	0	1	1	0	0	1	0
---	---	---	---	---	---	---	---

bit addr
----------

# Appendix A : Instruction Set (9/19)

**RL      A**

## Rotate Accumulator Left

**Operation :**       $(A_{n+1}) \leftarrow (A_n)$        $n=0\sim6$   
                           $(A_0) \leftarrow (A_7)$

**Encoding :**      HEX: 23h, #bytes: 1, Cycles: 1

0	0	1	0	0	0	1	1
---	---	---	---	---	---	---	---

**RLC     A**

## Rotate Accumulator Left through the Carry flag

**Operation :**       $(A_{n+1}) \leftarrow (A_n)$        $n=0\sim6$   
                           $(A_0) \leftarrow (C)$   
                           $(C) \leftarrow (A_7)$

**Encoding :**      HEX: 33h, #bytes: 1, Cycles: 1

0	0	1	1	0	0	1	1
---	---	---	---	---	---	---	---

**RR      A**

## Rotate Accumulator Right

**Operation :**       $(A_n) \leftarrow (A_{n+1})$        $n=0\sim6$   
                           $(A_7) \leftarrow (A_0)$

**Encoding :**      HEX: 03h, #bytes: 1, Cycles: 1

0	0	0	0	0	0	1	1
---	---	---	---	---	---	---	---

**RRC     A**

## Rotate Accumulator Right through the Carry flag

**Operation :**       $(A_n) \leftarrow (A_{n+1})$        $n=0\sim6$   
                           $(A_7) \leftarrow (C)$   
                           $(C) \leftarrow (A_0)$

**Encoding :**      HEX: 13h, #bytes: 1, Cycles: 1

0	0	0	1	0	0	1	1
---	---	---	---	---	---	---	---

**SWAP    A**

## Swap nibbles within the Accumulator

**Operation :**       $(A_{3-0}) \leftrightarrow (A_{7-4})$

**Encoding :**      HEX: C4h, #bytes: 1, Cycles: 1

1	1	0	0	0	1	0	0
---	---	---	---	---	---	---	---

# Appendix A : Instruction Set (10/19)

**MOV** <dest-byte>, <src-byte>

## Move byte variable

MOV	A, Rn
<b>Operation :</b>	(A) ← (Rn)
MOV	A, @Ri
<b>Operation :</b>	(A) ← ((Ri))
MOV	A, direct
<b>Operation :</b>	(A) ← (direct)
MOV	A, #date
<b>Operation :</b>	(A) ← data
MOV	Rn, A
<b>Operation :</b>	(Rn) ← (A)
MOV	Rn, direct
<b>Operation :</b>	(Rn) ← (direct)
MOV	Rn, #date
<b>Operation :</b>	(Rn) ← data
MOV	direct, A
<b>Operation :</b>	(direct) ← (A)
MOV	direct, Rn
<b>Operation :</b>	(direct) ← (Rn)

**Encoding :** HEX: E8h, #bytes: 1, Cycles: 1

1 1 1 0 1 r r r

**Encoding :** HEX: E6h, #bytes: 1, Cycles: 1

1 1 1 0 0 1 1 i

**Encoding :** HEX: E5h, #bytes: 2, Cycles: 2

1 1 1 0 0 1 0 1

direct addr

**Encoding :** HEX: 74h, #bytes: 2, Cycles: 2

0 1 1 1 0 1 0 0

immediate data

**Encoding :** HEX: F8h, #bytes: 1, Cycles: 1

1 1 1 1 1 r r r

**Encoding :** HEX: A8h, #bytes: 2, Cycles: 2

1 0 1 0 1 r r r

direct addr

**Encoding :** HEX: 78h, #bytes: 2, Cycles: 2

0 1 1 1 1 r r r

immediate data

**Encoding :** HEX: F5h, #bytes: 2, Cycles: 2

1 1 1 1 0 1 0 1

direct addr

**Encoding :** HEX: 88h, #bytes: 2, Cycles: 2

1 0 0 0 1 r r r

direct addr

# Appendix A : Instruction Set (11/19)

MOV	direct, @Ri
<b>Operation :</b>	(direct) ← ((Ri))
MOV	direct, direct
<b>Operation :</b>	(direct) ← (direct)
MOV	direct, #data
<b>Operation :</b>	(direct) ← data
MOV	@Ri, A
<b>Operation :</b>	((Ri)) ← (A)
MOV	@Ri, direct
<b>Operation :</b>	((Ri)) ← (direct)
MOV	@Ri, #data
<b>Operation :</b>	((Ri)) ← data

**MOV <dest-bit>, <src-bit>**

## Move bit data

MOV	C, bit
<b>Operation :</b>	(C) ← (bit)
MOV	bit, C
<b>Operation :</b>	(bit) ← (C)

**Encoding :** HEX: 86h, #bytes: 2, Cycles: 2

1	0	0	0	0	1	1	i	direct addr
---	---	---	---	---	---	---	---	-------------

**Encoding :** HEX: 85h, #bytes: 3, Cycles: 3

1	0	0	0	0	1	0	1	direct addr(src)	direct addr(dest)
---	---	---	---	---	---	---	---	------------------	-------------------

**Encoding :** HEX: 75h, #bytes: 3, Cycles: 3

0	1	1	1	0	1	0	1	direct addr	immediate data
---	---	---	---	---	---	---	---	-------------	----------------

**Encoding :** HEX: F6h, #bytes: 1, Cycles: 1

1	1	1	1	0	1	1	i
---	---	---	---	---	---	---	---

**Encoding :** HEX: A6h, #bytes: 2, Cycles: 2

1	0	1	0	0	1	1	i	direct addr
---	---	---	---	---	---	---	---	-------------

**Encoding :** HEX: 76h, #bytes: 2, Cycles: 2

0	1	1	1	0	1	1	i	immediate Data
---	---	---	---	---	---	---	---	----------------

**Encoding :** HEX: A2h, #bytes: 2, Cycles: 2

1	0	1	0	0	0	1	0	bit addr
---	---	---	---	---	---	---	---	----------

**Encoding :** HEX: 92h, #bytes: 2, Cycles: 2

1	0	0	1	0	0	1	0	bit addr
---	---	---	---	---	---	---	---	----------

# Appendix A : Instruction Set (12/19)

**MOV DPTR, #data16**

## Load Data Pointer with a 16-bit constant

**Operation :** (DPTR)  $\leftarrow$  data<sub>15-0</sub>  
(DPH, DPL)  $\leftarrow$  (data<sub>15-8</sub>, data<sub>7-0</sub>)

**Encoding :** HEX: 90h, #bytes: 3, Cycles: 3

1	0	0	1	0	0	0	0	immed. data 15-8	immed. data 7-0
---	---	---	---	---	---	---	---	------------------	-----------------

**MOVC A, @A + <base-reg>**

## Move Code byte

**MOVC A, @A + DPTR**

**Operation :** (A)  $\leftarrow$  ((A) + (DPTR))

**Encoding :** HEX: 93h, #bytes: 1, Cycles: 2

1	0	0	1	0	0	1	1
---	---	---	---	---	---	---	---

**MOVC A, @A + PC**

**Operation :** (PC)  $\leftarrow$  (PC) + 1  
(A)  $\leftarrow$  ((A) + (PC))

**Encoding :** HEX: 83h, #bytes: 1, Cycles: 2

1	0	0	0	0	0	1	1
---	---	---	---	---	---	---	---

**MOVX <dest-byte>, <src-byte>**

## Move External

**MOVX A, @Ri**

**Operation :** (A)  $\leftarrow$  ((Ri))

**Encoding :** HEX: E2h, #bytes: 1, Cycles: 3

1	1	1	0	0	0	1	i
---	---	---	---	---	---	---	---

**MOVX A, @DPTR**

**Operation :** (A)  $\leftarrow$  ((DPTR))

**Encoding :** HEX: E0h, #bytes: 1, Cycles: 3

1	1	1	0	0	0	0	0
---	---	---	---	---	---	---	---

**MOVX @Ri, A**

**Operation :** ((Ri))  $\leftarrow$  (A)

**Encoding :** HEX: F2h, #bytes: 1, Cycles: 3

1	1	1	1	0	0	1	i
---	---	---	---	---	---	---	---

**MOVX @DPTR, A**

**Operation :** ((DPTR))  $\leftarrow$  (A)

**Encoding :** HEX: F0h, #bytes: 1, Cycles: 3

1	1	1	1	0	0	0	0
---	---	---	---	---	---	---	---

# Appendix A : Instruction Set (13/19)

**XCH**    **A, <src-byte>**

**Exchange Accumulator with byte variable**

**XCH**    **A, Rn**

**Operation :**    (A) ↔ (Rn)

**XCH**    **A, @Ri**

**Operation :**    (A) ↔ ((Ri))

**XCH**    **A, direct**

**Operation :**    (A) ↔ (direct)

**Encoding :**    **HEX: C8h, #bytes: 1, Cycles: 1**

1	1	0	0	1	r	r	r
---	---	---	---	---	---	---	---

**Encoding :**    **HEX: C6h, #bytes: 1, Cycles: 1**

1	1	0	0	0	1	1	i
---	---	---	---	---	---	---	---

**Encoding :**    **HEX: C5h, #bytes: 2, Cycles: 2**

1	1	0	0	0	1	0	1	direct addr
---	---	---	---	---	---	---	---	-------------

**XCHD**    **A, @Ri**

**Exchange Digit**

**Operation :**    (A<sub>3-0</sub>) ↔ ((Ri))<sub>3-0</sub>

**Encoding :**    **HEX: D6h, #bytes: 1, Cycles: 1**

1	1	0	1	0	1	1	i
---	---	---	---	---	---	---	---

**PUSH**    **direct**

**Push onto stack**

**Operation :**    (SP) ← (SP) + 1  
                   ((SP)) ← (direct)

**Encoding :**    **HEX: C0h, #bytes: 2, Cycles: 2**

1	1	0	0	0	0	0	0	direct addr
---	---	---	---	---	---	---	---	-------------

**POP**    **direct**

**Pop onto stack**

**Operation :**    (direct) ← ((SP))  
                   (SP)    ← (SP) - 1

**Encoding :**    **HEX: D0h, #bytes: 2, Cycles: 2**

1	1	0	1	0	0	0	0	direct addr
---	---	---	---	---	---	---	---	-------------

# Appendix A : Instruction Set (14/19)

**SETB** <bit>

**Set bit**

**SETB** C

**Operation :** (C)  $\leftarrow$  1

**SETB** bit

**Operation :** (bit)  $\leftarrow$  1

**JC** rel

**Jump if Carry is set**

**Operation :** (PC)  $\leftarrow$  (PC) + 2  
If (C) = 1, then (PC)  $\leftarrow$  (PC) + rel

**JNC** rel

**Jump if Carry is not set**

**Operation :** (PC)  $\leftarrow$  (PC) + 2  
If (C) = 0, then (PC)  $\leftarrow$  (PC) + rel

**JB** bit, rel

**Jump if Bit is set**

**Operation :** (PC)  $\leftarrow$  (PC) + 3  
If (bit) = 1, then (PC)  $\leftarrow$  (PC)+rel

**JNB** bit, rel

**Jump if Bit is not set**

**Operation :** (PC)  $\leftarrow$  (PC) + 3  
If (bit) = 0, then (PC)  $\leftarrow$  (PC)+rel

**Encoding :** HEX: D3h, #bytes: 1, Cycles: 1

1 1 0 1 0 0 1 1

**Encoding :** HEX: D2h, #bytes: 2, Cycles: 2

1 1 0 1 0 0 1 0

bit addr

**Encoding :** HEX: 40h, #bytes: 2, Cycles: 3

0 1 0 0 0 0 0 0

relative addr

**Encoding :** HEX: 50h, #bytes: 2, Cycles: 3

0 1 0 1 0 0 0 0

relative addr

**Encoding :** HEX: 20h, #bytes: 3, Cycles: 4

0 0 1 0 0 0 0 0

bit addr

relative addr

**Encoding :** HEX: 30h, #bytes: 3, Cycles: 4

0 0 1 1 0 0 0 0

bit addr

relative addr

# Appendix A : Instruction Set (15/19)

**JBC bit, rel**

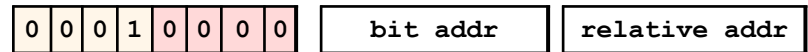
**Jump if Bit is set and Clear bit**

**Operation :**

$$(PC) \leftarrow (PC) + 3$$

If (bit) = 1,  
then (bit)  $\leftarrow$  0, (PC)  $\leftarrow$  (PC) + rel

**Encoding :** HEX: 10h, #bytes: 3, Cycles: 4



**ACALL addr11**

**Absolute Subroutine Call**

**Operation :**

$$(PC) \leftarrow (PC) + 2$$

$$(SP) \leftarrow (SP) + 1$$

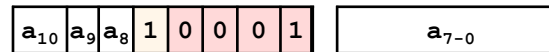
$$((SP)) \leftarrow (PC_{7-0})$$

$$(SP) \leftarrow (SP) + 1$$

$$((SP)) \leftarrow (PC_{15-8})$$

$$(PC_{10-0}) \leftarrow \text{page address}$$

**Encoding :** HEX: 11h, #bytes: 2, Cycles: 3



**LCALL addr16**

**Long Subroutine Call**

**Operation :**

$$(PC) \leftarrow (PC) + 3$$

$$(SP) \leftarrow (SP) + 1$$

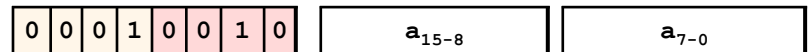
$$((SP)) \leftarrow (PC_{7-0})$$

$$(SP) \leftarrow (SP) + 1$$

$$((SP)) \leftarrow (PC_{15-8})$$

$$(PC) \leftarrow \text{addr}_{15-0}$$

**Encoding :** HEX: 12h, #bytes: 3, Cycles: 4



# Appendix A : Instruction Set (16/19)

## RET

### Return from Subroutine

**Operation :**

$$\begin{aligned} (PC_{15-8}) &\leftarrow ((SP)) \\ (SP) &\leftarrow (SP) - 1 \\ (PC_{7-0}) &\leftarrow ((SP)) \\ (SP) &\leftarrow (SP) - 1 \end{aligned}$$

**Encoding :** HEX: 22h, #bytes: 1, Cycles: 2

0	0	1	0	0	0	1	0
---	---	---	---	---	---	---	---

## RETI

### Return from Interrupt

**Operation :**

$$\begin{aligned} (PC_{15-8}) &\leftarrow ((SP)) \\ (SP) &\leftarrow (SP) - 1 \\ (PC_{7-0}) &\leftarrow ((SP)) \\ (SP) &\leftarrow (SP) - 1 \end{aligned}$$

**Encoding :** HEX: 32h, #bytes: 1, Cycles: 2

0	0	1	1	0	0	1	0
---	---	---	---	---	---	---	---

## AJMP addr11

### Absolute Jump

**Operation :**

$$\begin{aligned} (PC) &\leftarrow (PC) + 2 \\ (PC_{10-0}) &\leftarrow \text{page address} \end{aligned}$$

**Encoding :** HEX: 01h, #bytes: 2, Cycles: 3

a <sub>10</sub>	a <sub>9</sub>	a <sub>8</sub>	0	0	0	0	1	a <sub>7-0</sub>
-----------------	----------------	----------------	---	---	---	---	---	------------------

## SJMP rel

### Short Jump (Relative address)

**Operation :**

$$\begin{aligned} (PC) &\leftarrow (PC) + 2 \\ (PC_{10-0}) &\leftarrow (PC) + \text{rel} \end{aligned}$$

**Encoding :** HEX: 80h, #bytes: 2, Cycles: 3

1	0	0	0	0	0	0	0	relative addr
---	---	---	---	---	---	---	---	---------------

## LJMP addr16

### Long Jump

**Operation :** (PC)  $\leftarrow$  addr<sub>15-0</sub>

**Encoding :** HEX: 02h, #bytes: 3, Cycles: 4

0	0	0	0	0	0	1	0	a <sub>15-8</sub>	a <sub>7-0</sub>
---	---	---	---	---	---	---	---	-------------------	------------------

# Appendix A : Instruction Set (17/19)

**JMP @A + DPTR**

**Jump Indirect Relative to the DPTR**

**Operation :** (PC)  $\leftarrow$  (A) + (DPTR)

**Encoding :** HEX: 73h, #bytes: 1, Cycles: 2

0	1	1	1	0	0	1	1
---	---	---	---	---	---	---	---

**JZ rel**

**Jump if Accumulator is Zero**

**Operation :** (PC)  $\leftarrow$  (PC) + 2  
If (A)=0, then (PC)  $\leftarrow$  (PC) + rel

**Encoding :** HEX: 60h, #bytes: 2, Cycles: 3

0	1	1	0	0	0	0	0
---	---	---	---	---	---	---	---

relative addr
---------------

**JNZ rel**

**Jump if Accumulator is Not Zero**

**Operation :** (PC)  $\leftarrow$  (PC) + 2  
If (A) $\neq$ 0, then (PC)  $\leftarrow$  (PC) + rel

**Encoding :** HEX: 70h, #bytes: 2, Cycles: 3

0	1	1	1	0	0	0	0
---	---	---	---	---	---	---	---

relative addr
---------------

# Appendix A : Instruction Set (18/19)

**CJNE** <dest-byte>, <src-byte>, rel

## Compare and Jump if Not Equal

**CJNE** A, direct, rel

(PC)  $\leftarrow$  (PC) + 3  
 If (A)  $\neq$  (direct),  
 then (PC)  $\leftarrow$  (PC) + rel  
 If (A) < (direct), then (C)  $\leftarrow$  1  
 Else (C)  $\leftarrow$  0

**CJNE** A, #data, rel

(PC)  $\leftarrow$  (PC) + 3  
 If (A)  $\neq$  data,  
 then (PC)  $\leftarrow$  (PC) + rel  
 If (A) < data, then (C)  $\leftarrow$  1  
 Else (C)  $\leftarrow$  0

**CJNE** Rn, #data, rel

(PC)  $\leftarrow$  (PC) + 3  
 If (Rn)  $\neq$  data,  
 then (PC)  $\leftarrow$  (PC) + rel  
 If (Rn) < data, then (C)  $\leftarrow$  1  
 Else (C)  $\leftarrow$  0

**CJNE** @Ri, #data, rel

(PC)  $\leftarrow$  (PC) + 3  
 If ((Ri))  $\neq$  data,  
 then (PC)  $\leftarrow$  (PC) + rel  
 If ((Ri)) < data, then (C)  $\leftarrow$  1  
 Else (C)  $\leftarrow$  0

**Encoding :** HEX: B5h, #bytes: 3, Cycles: 4

1	0	1	1	0	1	0	1	direct addr	relative addr
---	---	---	---	---	---	---	---	-------------	---------------

**Encoding :** HEX: B4h, #bytes: 3, Cycles: 4

1	0	1	1	0	1	0	0	immediate data	relative addr
---	---	---	---	---	---	---	---	----------------	---------------

**Encoding :** HEX: B8h, #bytes: 3, Cycles: 4

1	0	1	1	1	r	r	r	immediate data	relative addr
---	---	---	---	---	---	---	---	----------------	---------------

**Encoding :** HEX: B6h, #bytes: 3, Cycles: 4

1	0	1	1	0	1	1	i	immediate data	relative addr
---	---	---	---	---	---	---	---	----------------	---------------

# Appendix A : Instruction Set (19/19)

DJNZ <byte>, rel

## Decrement and Jump if Not Zero

DJNZ Rn, rel

**Operation :**  
(PC) ← (PC) + 2  
(Rn) ← (Rn) - 1  
If (Rn) ≠ 0, then (PC) ← (PC) + rel

**Encoding :** HEX: D8h, #bytes: 2, Cycles: 3

1	1	0	1	1	r	r	r	relative addr
---	---	---	---	---	---	---	---	---------------

DJNZ direct, rel

**Operation :**  
(PC) ← (PC) + 3  
(direct) ← (direct) - 1  
If (direct) ≠ 0,  
then (PC) ← (PC) + rel

**Encoding :** HEX: D5h, #bytes: 3, Cycles: 4

1	1	0	1	0	1	0	1	direct addr	relative addr
---	---	---	---	---	---	---	---	-------------	---------------

NOP

## No Operation

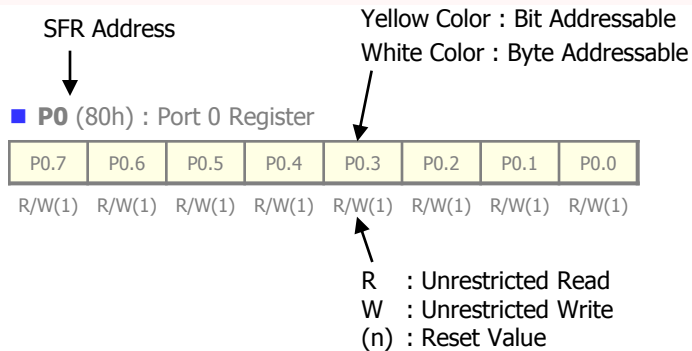
**Operation :** (PC) ← (PC) + 1

**Encoding :** HEX: 00h, #bytes: 1, Cycles: 1

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

# Appendix B : SFR Description [80h ~ 87h] (1/12)

## [How to Read a SFR Descriptions]



### ■ **P0** (80h) : Port 0 Register

P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ◆ Port 0 Register

### ■ **SP** (81h) : Stack Pointer Register

SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(1)

- ◆ Indicate where stack will start.
- ◆ Increment by PUSH and decrement by POP.

### ■ **DPL** (82h) : Data Pointer Low Register

DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

### ■ **DPH** (83h) : Data Pointer High Register

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

### ■ **PCON** (87h) : Power Control Register

SMOD1	-	-	POF	GF1	GF0	PD	IDL
R/W(0)			R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ SMOD1 : Timer 1 baudrate double in UART mode 1.
- ◆ POF : Power off flag.  
When power-on, this bit will be set by H/W.
- ◆ GF1, GF0 : General purpose flag bit.
- ◆ PD : Power-down (Stop) mode enable.
- ◆ IDL : IDLE mode enable.

# Appendix B : SFR Description [88h ~ 90h] (2/12)

## ■ TCON (88h) : Timer/Counter 0/1 Control Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
-----	-----	-----	-----	-----	-----	-----	-----

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ TF1 : Timer 1 overflow flag.
- ◆ TR1 : Timer 1 run enable.
- ◆ TF0 : Timer 0 overflow flag.
- ◆ TR0 : Timer 0 run enable.
- ◆ IE1 : External interrupt 1 flag.  
If IT1 = 0, cleared by S/W (software).  
If IT1 = 1, cleared automatically when go to routine.
- ◆ IT1 : External interrupt 1 type select flag.  
Edge detect (IT1=1) / Level detect (IT1=0; Default)
- ◆ IE0 : External interrupt 0 flag.  
If IT0 = 0, cleared by S/W (software).  
If IT0 = 1, cleared automatically when go to routine.
- ◆ IT0 : External interrupt 0 type select flag.  
Edge detect (IT0=1) / Level detect (IT0=0; Default)

## ■ TMOD (89h) : Timer/Counter 0 Mode Control Register

-	-	-	-	GATE	C/T	M1	M0
---	---	---	---	------	-----	----	----

R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ GATE[3] : Timer 0 gate control.
- ◆ C/T[2] : Timer 0 Counter/Timer select.  
0 = Timer by  $F_{osc}/12$ . (Default)  
1 = Counter by T0 pin.
- ◆ M1, M0 : Timer 0 mode selection.  
[0,0] : Mode0, 13-bit T/C  
[0,1] : Mode1, 16-bit T/C  
[1,0] : Mode2, 8-bit T/C with auto-reload  
[1,1] : Mode3, Two 8-bit T/C

## ■ TLO (8Ah) : Timer/Counter 0 Low Byte Register

TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## ■ TL1 (8Bh) : Timer/Counter 1 Low Byte Register

TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## ■ TH0 (8Ch) : Timer/Counter 0 High Byte Register

TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## ■ TH1 (8Dh) : Timer/Counter 1 High Byte Register

TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
-------	-------	-------	-------	-------	-------	-------	-------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## ■ P1 (90h) : Port 1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
------	------	------	------	------	------	------	------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ◆ P1.0 : XTAL 1 alternative. (Default = XTAL1).
- ◆ P1.1 : XTAL 2 alternative. (Default = XTAL2).  
Refer to ALTSEL & PMR SFR for I/O pins.
- ◆ P1.2 : RESETB alternative. (Default = RESETB)  
Refer to ALTSEL for I/O Pins.

# Appendix B : SFR Description [91h ~ 95h] (3/12)

## ■ EXIF (91h) : External Interrupt Flag Register

-	-	IE3	IE2	XT/RG	RGMD	RGSL	BGS
R/W(0)	R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(1)		

- ◆ IE3 : External interrupt 3 flag. Cleared by S/W.
- ◆ IE2 : External interrupt 2 flag. Cleared by S/W.
- ◆ XT/RG : System clock selection.  
0 = Internal Ring oscillator is selected as system clock.  
1 = External clock is selected as system clock.
- ◆ RGMD : Ring mode. Now system clock is Ring or XTAL.  
Generally RGMD is the invert of XT/RG.
- ◆ RGSL : Ring select bit when power-down wake-up.  
1 = When wake-up from power-down mode in XTAL clock, use Ring oscillator as system clock during 65,536 XTAL clocks.
- ◆ BGS : Band-gap select. (Default = 1)  
0 = Band-gap block (LVD) will do not run in power-down mode, but function during normal mode.  
It will support the significant power savings in power-down mode.  
1 = Band-gap block (LVD) will run in power-down mode.

## ■ CLKOFF (94h) : Peripheral Clock Control Register

-	-	OFF_T01	OFF_UART	-	OFF_I2C	OFF_PWM	OFF_ADC
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ OFF\_ADC : ADC block OFF. 1 = ADC block will stop.
- ◆ OFF\_PWM : PWM block OFF. 1 = PWM block will stop.
- ◆ OFF\_I2C : I<sup>2</sup>C block OFF. 1 = I<sup>2</sup>C Master & Slave block will stop.
- ◆ OFF\_UART : UART block OFF. 1 = UART block will stop.
- ◆ OFF\_T01 : Timer0/1 block OFF. 1 = Timer0 and Timer1 will stop.

## ■ RINGCON (95h) : Ring Control Configuration Register

S7	S6	S5	S4	S3	S2	S1	S0
R/W(0)	R/W(10)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ RINGCON[7:0] : Internal Ring OSC. can be tuned.

# Appendix B : SFR Description [96h ~ 9Ah] (4/12)

## ■ LVDCON (96h) : LVD Control Register

-	-	-	-	-	LVDCON.2	LVDCON.1	LVDCON.0
					R/W(0)	R/W(0)	R/W(0)

- ◆ LVDCON[2:0] : Select the interrupt level of LVD.
- ◆ LVDCON[2:0] = 000b, LVD interrupt level = 4.0V (default)
- ◆ LVDCON[2:0] = 001b, LVD interrupt level = 3.6V
- ◆ LVDCON[2:0] = 010b, LVD interrupt level = 3.2V
- ◆ LVDCON[2:0] = 011b, LVD interrupt level = 3.0V
- ◆ LVDCON[2:0] = 100b, LVD interrupt level = 2.8V
- ◆ LVDCON[2:0] = 101b, LVD interrupt level = 2.6V
- ◆ LVDCON[2:0] = 110b, LVD interrupt level = 2.4V
- ◆ LVDCON[2:0] = 111b, LVD interrupt level = 2.2V

## ■ LVDST (97h) : LVD Status Register

LVD7	LVD6	LVD5	LVD4	LVD3	LVD2	LVD1	LVD0
R(0)	R(0)	R(0)	R(0)	R(0)	R(0)	R(0)	R(0)

- ◆ LVD7 = 1 when VDD ≤ 4.0V
- ◆ LVD6 = 1 when VDD ≤ 3.6V
- ◆ LVD5 = 1 when VDD ≤ 3.2V
- ◆ LVD4 = 1 when VDD ≤ 3.0V
- ◆ LVD3 = 1 when VDD ≤ 2.8V
- ◆ LVD2 = 1 when VDD ≤ 2.6V
- ◆ LVD1 = 1 when VDD ≤ 2.4V
- ◆ LVD0 = 1 when VDD ≤ 2.2V

## ■ SCON (98h) : Serial Port Control Register of UART0

-	-	-	REN	-	-	TI	RI
			R/W(0)			R/W(0)	R/W(0)

- ◆ REN : Serial reception enable.
- ◆ TI : Transmission interrupt flag. Must be cleared by S/W.
- ◆ RI : Reception interrupt flag. Must be cleared by S/W.

## ■ SBUF (99h) : Serial Data Buffer Register

SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ Transmission buffer and reception buffer are separated.
- ◆ Read and write address are same.

## ■ I2C\_SCON (9Ah) : I<sup>2</sup>C Slave Control Register

-	WR	RD	BUSY	-	I2C_SIF	MODE	RUN
	R(0)	R(0)	R(0)		R/W(0)	R/W(0)	R/W(0)

- ◆ WR : I<sup>2</sup>C write operation status. Cleared by H/W.
- ◆ RD : I<sup>2</sup>C read operation status. Cleared by H/W.
- ◆ BUSY : Current I<sup>2</sup>C slave status. Cleared by H/W.  
1 = I<sup>2</sup>C slave is running now.
- ◆ I2C\_SCIF: I<sup>2</sup>C slave interrupt flag.  
It is set each time a byte is received or transmitted.  
Cleared by S/W.
- ◆ MODE : I<sup>2</sup>C slave Mode.  
0 = Mode 0. Including memory address (default).  
1 = Mode 1. no memory address.
- ◆ RUN : I<sup>2</sup>C slave start.  
Cleared by S/W.

# Appendix B : SFR Description [9Bh ~ A4h] (5/12)

## ■ I2C\_SDEV (9Bh) : I<sup>2</sup>C Slave Device Address Register

SDEV.7	SDEV.6	SDEV.5	SDEV.4	SDEV.3	SDEV.2	SDEV.1	SDEV.0
--------	--------	--------	--------	--------	--------	--------	--------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ SDEV[7:1] : I<sup>2</sup>C slave device address.
- ◆ SDEV[0] : Not used. Don't care.

## ■ I2C\_SADR (9Ch) : I<sup>2</sup>C Slave Memory Address Register

SADR.7	SADR.6	SADR.5	SADR.4	SADR.3	SADR.2	SADR.1	SADR.0
--------	--------	--------	--------	--------	--------	--------	--------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## ■ I2C\_SDAT (9Dh) : I<sup>2</sup>C Slave Data Register

SDAT.7	SDAT.6	SDAT.5	SDAT.4	SDAT.3	SDAT.2	SDAT.1	SDAT.0
--------	--------	--------	--------	--------	--------	--------	--------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## ■ I2C\_MDAT (9Eh) : I<sup>2</sup>C Master Data Register

MDAT.7	MDAT.6	MDAT.5	MDAT.4	MDAT.3	MDAT.2	MDAT.1	MDAT.0
--------	--------	--------	--------	--------	--------	--------	--------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## ■ P2 (A0h) : Port 2 Register

P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
------	------	------	------	------	------	------	------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ◆ Port 2 Register

## ■ I2C\_MCON (A2h) : I<sup>2</sup>C Master Control Register

-	-	-	I2C_MIF	OP	BYPASS	MODE	RUN
---	---	---	---------	----	--------	------	-----

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ I2C\_MIF : I<sup>2</sup>C Master interrupt flag.  
It is set each time a byte is received or transmitted.  
Cleared by S/W.
- ◆ OP : I<sup>2</sup>C read/write operation.  
0 = write operation  
1 = read operation
- ◆ BYPASS : Bypass Mode in I<sup>2</sup>C master and slave.
- ◆ MODE : I<sup>2</sup>C master Mode.  
0 = Mode 0 including memory address (default)  
1 = Mode 1. no memory address
- ◆ RUN : I<sup>2</sup>C master start.  
Cleared by H/W.

## ■ I2C\_MDEV (A3h) : I<sup>2</sup>C Master Device Address Register

MDEV.7	MDEV.6	MDEV.5	MDEV.4	MDEV.3	MDEV.2	MDEV.1	MDEV.0
--------	--------	--------	--------	--------	--------	--------	--------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## ■ I2C\_MADR (A4h) : I<sup>2</sup>C Master Memory Address Register

MADR.7	MADR.6	MADR.5	MADR.4	MADR.3	MADR.2	MADR.1	MADR.0
--------	--------	--------	--------	--------	--------	--------	--------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

# Appendix B : SFR Description [A5h ~ B8h] (6/12)

## ■ I2C\_MNUM (A5h) : I<sup>2</sup>C Master Multi-byte Number Register

MNUM.7	MNUM.6	MNUM.5	MNUM.4	MNUM.3	MNUM.2	MNUM.1	MNUM.0
--------	--------	--------	--------	--------	--------	--------	--------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

◆ Number of multi-byte = I2C\_MNUM + 1

## ■ I2C\_MSCL (A6h) : I<sup>2</sup>C Master Clock Scale Factor Low Byte Register

MSCL.7	MSCL.6	MSCL.5	MSCL.4	MSCL.3	MSCL.2	MSCL.1	MSCL.0
--------	--------	--------	--------	--------	--------	--------	--------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

◆ Frequency of I<sup>2</sup>C Master ( $F_{I2C}$ ) =  $F_{OSC} / \{(I2C_MSCH, I2C_MSCL)*4\}$

## ■ I2C\_MSCH (A7h) : I<sup>2</sup>C Master Clock Scale Factor High Byte Register

MSCH.7	MSCH.6	MSCH.5	MSCH.4	MSCH.3	MSCH.2	MSCH.1	MSCH.0
--------	--------	--------	--------	--------	--------	--------	--------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

## ■ IE (A8h) : Interrupt Enable Register

EA	EADC	-	ES	ET1	EX1	ET0	EX0
----	------	---	----	-----	-----	-----	-----

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ EA : Global interrupt enable.
- ◆ EADC : ADC interrupt enable.
- ◆ ES : Serial port interrupt enable.
- ◆ ET1 : Timer 1 interrupt enable.
- ◆ EX1 : External interrupt 1 enable.
- ◆ ET0 : Timer0 interrupt enable.
- ◆ EX0 : External interrupt 0 enable.

## ■ P3 (B0h) : Port 3 Register

-	-	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
---	---	------	------	------	------	------	------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

◆ Port 3 Register

## ■ IP (B8h) : Interrupt Priority Register

-	PADC	-	PS	PT1	PX1	PT0	PX0
---	------	---	----	-----	-----	-----	-----

R(1) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ PADC : ADC interrupt priority.
- ◆ PS : Serial port interrupt priority.
- ◆ PT1 : Timer 1 interrupt priority.
- ◆ PX1 : External interrupt 1 priority.
- ◆ PT0 : Timer 0 interrupt priority.
- ◆ PX0 : External interrupt 0 priority.

# Appendix B : SFR Description [BEh ~ D0h] (7/12)

## ■ OSCICN (BEh) : Internal Ring Oscillator Control Register

-	-	-	-	DIV2	RINGON	DIV1	DIV0
				R/W(1)	R/W(1)	R/W(0)	R/W(0)

- ◆ RINGON : 1 = Internal ring oscillator is running.  
0 = Internal ring oscillator is killed.  
Don't clear RINGON bit when XTRG = 0.
- ◆ DIV2, DIV1, DIV0 : Ring oscillator divider.  
if Ring OSC. is 12MHz(@3V),
 

[0,0,0]	= 12MHz/1	( 12.0 MHz)
[0,0,1]	= 12MHz/2	( 6.0 MHz)
[0,1,0]	= 12MHz/4	( 3.0 MHz)
[0,1,1]	= 12MHz/8	( 1.5 MHz)
[1,0,0]	= 12MHz/3	( 4.0 MHz) (Default)
[1,0,1]	= 12MHz/6	( 2.0 MHz)
[1,1,0]	= 12MHz/12	( 1.0 MHz)
[1,1,1]	= Reserved.	

## ■ PMR (C4h) : Power Management Control Register

-	-	-	-	XTOFF	-	-	-
				R/W(0)			

- ◆ XTOFF : Internal amplifier disable for external crystal oscillator.  
1 = External crystal will be killed.  
0 = External crystal will run (Default).  
Don't set XTOFF bit when XT/RG = 1.

## ■ STATUS (C5h) : Crystal Status Register

-	-	-	XTUP	-	-	-	-
				R(0)			

- ◆ XTUP : Crystal oscillator warm-up status.  
It represents the crystal clock is stable (1) or not (0).  
Cleared by H/W when Power-on reset and all kinds of reset.  
Cleared by H/W when XTOFF bit is set.  
Cleared by during Power-down wake-up when XT/RG = 1.  
Set by H/W after XTAL stabilization time.

## ■ PSW (D0h) : Program Status Word Register

CY	AC	F0	RS1	RS0	OV	F1	P
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R(0)

- ◆ CY : Carry flag.
- ◆ AC : Auxiliary carry flag.
- ◆ F0 : User flag 0.
- ◆ RS1, RS0 : Register bank select.
 

[0,0]	: Bank 0	[1,0]	: Bank 2
[0,1]	: Bank 1	[1,1]	: Bank 3
- ◆ OV : Overflow flag.
- ◆ F1 : User flag 1.
- ◆ P : Parity bit. Set/clear by H/W according to ACC odd parity.

# Appendix B : SFR Description [D4h ~ DAh] (8/12)

## ■ P0TYPE (D4h) : Port 0 Type Control Register

P0TYPE.7	P0TYPE.6	P0TYPE.5	P0TYPE.4	P0TYPE.3	P0TYPE.2	P0TYPE.1	P0TYPE.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ 0 = Push-pull Output (Default) / 1 = Open-drain Output

## ■ P1TYPE (D5h) : Port 1 Type Control Register

P1TYPE.7	P1TYPE.6	P1TYPE.5	P1TYPE.4	P1TYPE.3	P1TYPE.2	P1TYPE.1	P1TYPE.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ 0 = Push-pull Output (Default) / 1 = Open-drain output

## ■ P2TYPE (D6h) : Port 2 Type Control Register

P2TYPE.7	P2TYPE.6	P2TYPE.5	P2TYPE.4	P2TYPE.3	P2TYPE.2	P2TYPE.1	P2TYPE.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ 0 = Push-pull Output (Default) / 1 = Open-drain Output

## ■ P3TYPE (D7h) : Port 3 Type Control Register

-	-	P3TYPE.5	P3TYPE.4	P3TYPE.3	P3TYPE.2	P3TYPE.1	P3TYPE.0
		R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ 0 = Push-pull Output (Default) / 1 = Open-drain Output

## ■ WDCON (D8h) : Watchdog Timer Control Register

WD1	WD0	EPFI	PFI	WDIF	WTRF	EWT	RWT
R/W(1)	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ WD1, WD0 : Watchdog timer mode select.
  - [0,0] : 1 x 2<sup>16</sup> clocks (interrupt) + 256 clocks (reset)
  - [0,1] : 4 x 2<sup>16</sup> clocks (interrupt) + 256 clocks (reset)
  - [1,0] : 16 x 2<sup>16</sup> clocks (interrupt) + 256 clocks (reset)
  - [1,1] : 32 x 2<sup>16</sup> clocks (interrupt) + 256 clocks (reset)
- ◆ EPFI : Power-fail interrupt enable.
- ◆ PFI : Power-fail interrupt flag.
- ◆ WDIF : Watchdog timer interrupt flag.
- ◆ WTRF : Watchdog timer reset flag. Cleared by S/W.
- ◆ EWT : Watchdog timer reset enable.
- ◆ RWT : Restart watchdog timer.

## ■ ADCHL (D9h) : ADC High Channel Selection Low Register

ADCH7B	ADCH6B	ADCH5B	ADCH4B	ADCH3B	ADCH2B	ADCH1B	ADCH0B
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ◆ ADCH<sub>X</sub>B = 0 : ADCH<sub>X</sub> input enable (Digital input disable)

## ■ ADCHH (DAh) : ADC High Channel Selection High Register

ADCH15B	ADCH14B	ADCH13B	ADCH12B	ADCH11B	ADCH10B	ADCH9B	ADCH8B
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ◆ ADCH<sub>X</sub>B = 0 : ADCH<sub>X</sub> input enable (Digital input disable)

# Appendix B : SFR Description [DBh ~ E1h] (9/12)

## ■ ADCHSEL (DBh) : ADC High Channel Selection Register

CH_SEL	-	-	-	CHH3	CHH2	CHH1	CHH0
R/W(0)				R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ CH\_SEL : ADC MUX Selector with CHH[3:0] & CH[3:0].  
0 = CH[3:0] → ADC[11:0] Enable / ADCH[15:0] Disable.  
1 = CHH[3:0] → ADC[11:0] Disable / ADCH[15:0] Enable.
- ◆ CHH[3:0] : ADC MUX Selection for High Channel (ADCH[15:0])
 

0000b : ADCH0 selection (0h)	1000b : ADCH8 selection (8h)
0001b : ADCH1 selection (1h)	1001b : ADCH9 selection (9h)
0010b : ADCH2 selection (2h)	1010b : ADCH10 selection (Ah)
0011b : ADCH3 selection (3h)	1011b : ADCH11 selection (Bh)
0100b : ADCH4 selection (4h)	1100b : ADCH12 selection (Ch)
0101b : ADCH5 selection (5h)	1101b : ADCH13 selection (Dh)
0110b : ADCH6 selection (6h)	1110b : ADCH14 selection (Eh)
0111b : ADCH7 selection (7h)	1111b : ADCH15 selection (Fh)

## ■ PWMCON (DCh) : PWM Control Register

POSEL	PS2_P0	PS1_P0	PS0_P0	-	PWMF	CLR_P0	RUN_P0
R/W(0)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)

- ◆ POSEL : PWM waveform output enable to P0.6.
- ◆ PS2\_P0, PS1\_P0, PS0\_P0 : Pre-scaled Clock Selection.  
 [0,0,0] =  $F_{osc}/1$ , [0,0,1] =  $F_{osc}/2$ , [0,1,0] =  $F_{osc}/4$ ,  
 [0,1,1] =  $F_{osc}/8$ , [1,0,0] =  $F_{osc}/16$ , [1,0,1] =  $F_{osc}/32$ ,  
 [1,1,0] =  $F_{osc}/64$ , [1,1,1] =  $F_{osc}/128$   
 \* PWM Clock ( $F_{pwm}$ ) to ADC should not be set to  $F_{osc}/1$ .
- ◆ PWMF : PWM interrupt flag. Cleared by S/W.
- ◆ CLR\_P0 : Counter reset enable. Cleared by H/W.
- ◆ RUN\_P0 : Counter start enable. PWM clock ( $F_{pwm}$ ) output enable.

## ■ PWMD (DEh) : PWM Duty Data Register

PWMD.7	PWMD.6	PWMD.5	PWMD.4	PWMD.3	PWMD.2	PWMD.1	PWMD.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

## ■ ACC/A (E0h) : Accumulator

ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

## ■ ADCSELH (E1h) : ADC Channel Selection High Register

ADC11B	ADC10B	ADC9B	ADC8B	ADC7B	ADC6B	ADC5B	ADC4B
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ◆ ADC11B : 0 = ADC11 input enable & digital input disable at P2.2.
- ◆ ADC10B : 0 = ADC10 input enable & digital input disable at P2.3.
- ◆ ADC9B : 0 = ADC9 input enable & digital input disable at P2.4.
- ◆ ADC8B : 0 = ADC8 input enable & digital input disable at P2.5.
- ◆ ADC7B : 0 = ADC7 input enable & digital input disable at P2.6.
- ◆ ADC6B : 0 = ADC6 input enable & digital input disable at P0.7.
- ◆ ADC5B : 0 = ADC5 input enable & digital input disable at P0.6.
- ◆ ADC4B : 0 = ADC4 input enable & digital input disable at P0.5.

# Appendix B : SFR Description [E2h ~ E6h] (10/12)

## ■ ADCSEL (E2h) : ADC Channel Selection Low & MUX Selection Register

ADC3B	ADC2B	ADC1B	ADC0B	CH3	Ch2	CH1	CH0
-------	-------	-------	-------	-----	-----	-----	-----

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

- ◆ ADC3B : 0 = ADC3 input enable & digital input disable at P0.4.
- ◆ ADC2B : 0 = ADC2 input enable & digital input disable at P0.3.
- ◆ ADC1B : 0 = ADC1 input enable & digital input disable at P0.2.
- ◆ ADC0B : 0 = ADC0 input enable & digital input disable at P0.1.

### ◆ CH[3:0] : ADC MUX Selection.

[0,0,0,0] = ADC0 selection (0h)

[0,0,0,1] = ADC1 selection (1h)

[0,0,1,0] = ADC2 selection (2h)

[0,0,1,1] = ADC3 selection (3h)

[0,1,0,0] = ADC4 selection (4h)

[0,1,0,1] = ADC5 selection (5h)

[0,1,1,0] = ADC6 selection (6h)

[0,1,1,1] = ADC7 selection (7h)

[1,0,0,0] = ADC8 selection (8h)

[1,0,0,1] = ADC9 selection (9h)

[1,0,1,0] = ADC10 selection (Ah)

[1,0,1,1] = ADC11 selection (Bh)

[1,1,0,0] = No ADC input select (Ch)

[1,1,0,1] = No ADC input select (Dh)

[1,1,1,0] = No ADC input select (Eh)

[1,1,1,1] = No ADC input select (Fh, Default)

## ■ ALTSEL (E3h) : Alternative Function Control Register

IOXEN	IORSTEN	CLO	PWM00	TVO	TX	-	-
-------	---------	-----	-------	-----	----	---	---

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ IOXEN : 1 = XTAL and XTAL2 is configured as I/O.  
Must be XTOFF (PMR.3) = 1 (Oscillator Amp. Off)
- ◆ IORSTEN : 1 = RESETB is configured as I/O.
- ◆ CLO : 1 = System clock output to P2.6.
- ◆ PWMD0 : 1 = PWM waveform output enable to P0.0.
- ◆ TVO : 1 = Timer 0 overflow clock to P0.0.
- ◆ TX : 1 = UART TX data output to P0.2.  
User must set TX bit to use UART.

## ■ POSEL (E4h) : Port 0 Pull-up Control Register

POSEL.7	POSEL.6	POSEL.5	POSEL.4	POSEL.3	POSEL.2	POSEL.1	POSEL.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ 0 = Pull-up resistor ON (Default)
- ◆ 1 = Pull-up resistor OFF when ADC\_EN (ADCON[7]) = 1

## ■ P1SEL (E5h) : Port 1 Pull-up Control Register

P1SEL.7	P1SEL.6	P1SEL.5	P1SEL.4	P1SEL.3	P1SEL.2	P1SEL.1	P1SEL.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(1) R/W(1)

- ◆ 0 = Pull-up resistor ON (Default)
- ◆ 1 = Pull-up resistor OFF when ADC\_EN (ADCON[7]) = 1

## ■ P2SEL (E6h) : Port 2 Pull-up Control Register

P2SEL.7	P2SEL.6	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	P2SEL.1	P2SEL.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ 0 = Pull-up resistor ON (Default)
- ◆ 1 = Pull-up resistor OFF when ADC\_EN (ADCON[7]) = 1

# Appendix B : SFR Description [E7h ~ F0h] (11/12)

## ■ P3SEL (E7h) : Port 3 Pull-up Control Register

-	-	P3SEL.5	P3SEL.4	P3SEL.3	P3SEL.2	P3SEL.1	P3SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ 0 = Pull-up resistor ON (Default)
- ◆ 1 = Pull-up resistor OFF when ADC\_EN (ADCON[7]) = 1

## ■ EIE (E8h) : Extended Interrupt Enable Register

-	-	EPWM	EWDT	EI2C_S	EI2C_M	EX3	EX2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ EPWM : PWM interrupt enable.
- ◆ EWDT : Watchdog interrupt enable.
- ◆ EI2C\_S : I<sup>2</sup>C slave interrupt enable.
- ◆ EI2C\_M : I<sup>2</sup>C master interrupt enable.
- ◆ EX3 : External 3 interrupt enable.
- ◆ EX2 : External 2 interrupt enable.

## ■ ADCR (EEh) : ADC Result High Register : Value[9:2]

SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

## ■ ADCON (EFh) : ADC Control & ADC Result Low Register : Value[1:0]

AD_EN	AD_REQ	AD_END	ADCF	-	ADIV	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)		R/W(0)	R/W(0)	R/W(0)

- ◆ AD\_EN : ADC ready enable.
- ◆ AD\_REQ : ADC start.  
Cleared by H/W when AD\_END goes to 1 from 0.
- ◆ AD\_END : Current ADC status.  
0 = ADC is running now.
- ◆ ADCF : ADC interrupt flag. Must be cleared by S/W.
- ◆ ADIV : ADC input clock select.  
0 = System clock ( $F_{OSC}$ ) / 2. (Default)  
1 = PWM input clock ( $F_{PWM}$ )
- ◆ SAR1, SAR0 : Low bits of ADC result value.

## ■ B (F0h) : B Register

B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

# Appendix B : SFR Description [F4h ~ FFh] (12/12)

## ■ P0DIR (F4h) : Port 0 Input/Output Control Register

P0DIR.7	P0DIR.6	P0DIR.5	P0DIR.4	P0DIR.3	P0DIR.2	P0DIR.1	P0DIR.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

◆ 1 = Input (Default) / 0 = Output

## ■ P1DIR (F5h) : Port 1 Input/Output Control Register

P1DIR.7	P1DIR.6	P1DIR.5	P1DIR.4	P1DIR.3	P1DIR.2	P1DIR.1	P1DIR.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

◆ 1 = Input (Default) / 0 = Output

## ■ P2DIR (F6h) : Port 2 Input/Output Control Register

P2DIR.7	P2DIR.6	P2DIR.5	P2DIR.4	P2DIR.3	P2DIR.2	P2DIR.1	P2DIR.0
---------	---------	---------	---------	---------	---------	---------	---------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

◆ 1 = Input (Default) / 0 = Output

## ■ P3DIR (F7h) : Port 3 Input/Output Control Register

-	-	P3DIR.5	P3DIR.4	P3DIR.3	P3DIR.2	P3DIR.1	P3DIR.0
---	---	---------	---------	---------	---------	---------	---------

R/W(1) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

◆ 1 = Input (Default) / 0 = Output

## ■ EIP (F8h) : Extended Interrupt Priority Register

-	-	PPWM	PWDT	PI2C_S	PI2C_M	PX3	PX2
---	---	------	------	--------	--------	-----	-----

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ PPWM : PWM interrupt priority bit.
- ◆ PWDT : Watchdog timer interrupt priority bit.
- ◆ PI2C\_S : I<sup>2</sup>C slave interrupt priority bit.
- ◆ PI2C\_M : I<sup>2</sup>C master interrupt priority bit.
- ◆ PX3 : External interrupt 3 priority bit.
- ◆ PX2 : External interrupt 2 priority bit.

## ■ EEAEN (FFh) : EEPROM Access Enable

-	-	-	-	-	-	-	EAEN
---	---	---	---	---	---	---	------

R/W(0)

- ◆ EAEN = 1, EEPROM access enable.

# Appendix C : Update History

## ◆ V1.0

- ✓ First Release.

## ◆ V1.3

- ✓ Update I<sup>2</sup>C Spec.

## ◆ V1.4

- ✓ Update I<sup>2</sup>C Spec.
- ✓ Update the External Reset slide.
- ✓ Update the 'IAP: Function Set' slide.
- ✓ Update the 'On-Chip POR' slide.
- ✓ Update the Product Numbering System
- ✓ Add a Package Type
  - 28 - SOIC

## ◆ V1.5

- ✓ Modify the Supply Voltage.
  - 2.4V ~ 5.5V
- ✓ Modify the Operating Temperature.
  - -40 °C to 120 °C

## ◆ V1.6

- ✓ Add on the Power Slope slide.

## ◆ V1.7

- ✓ Modify the Supply Voltage.
  - 2.2V ~ 5.5V

## ◆ V1.8

- ✓ Update stop current spec.
- ✓ Add on 32-QFN package